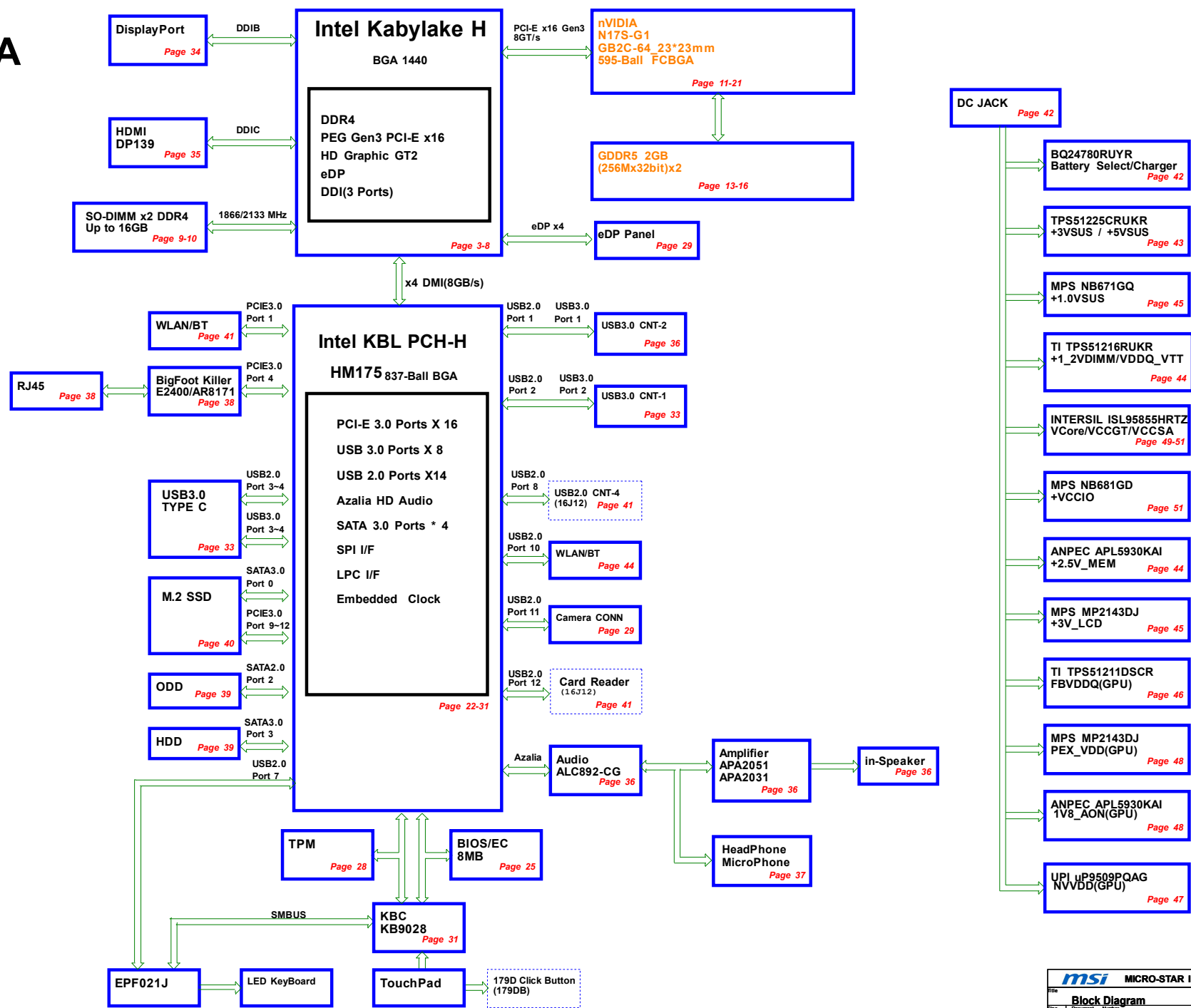
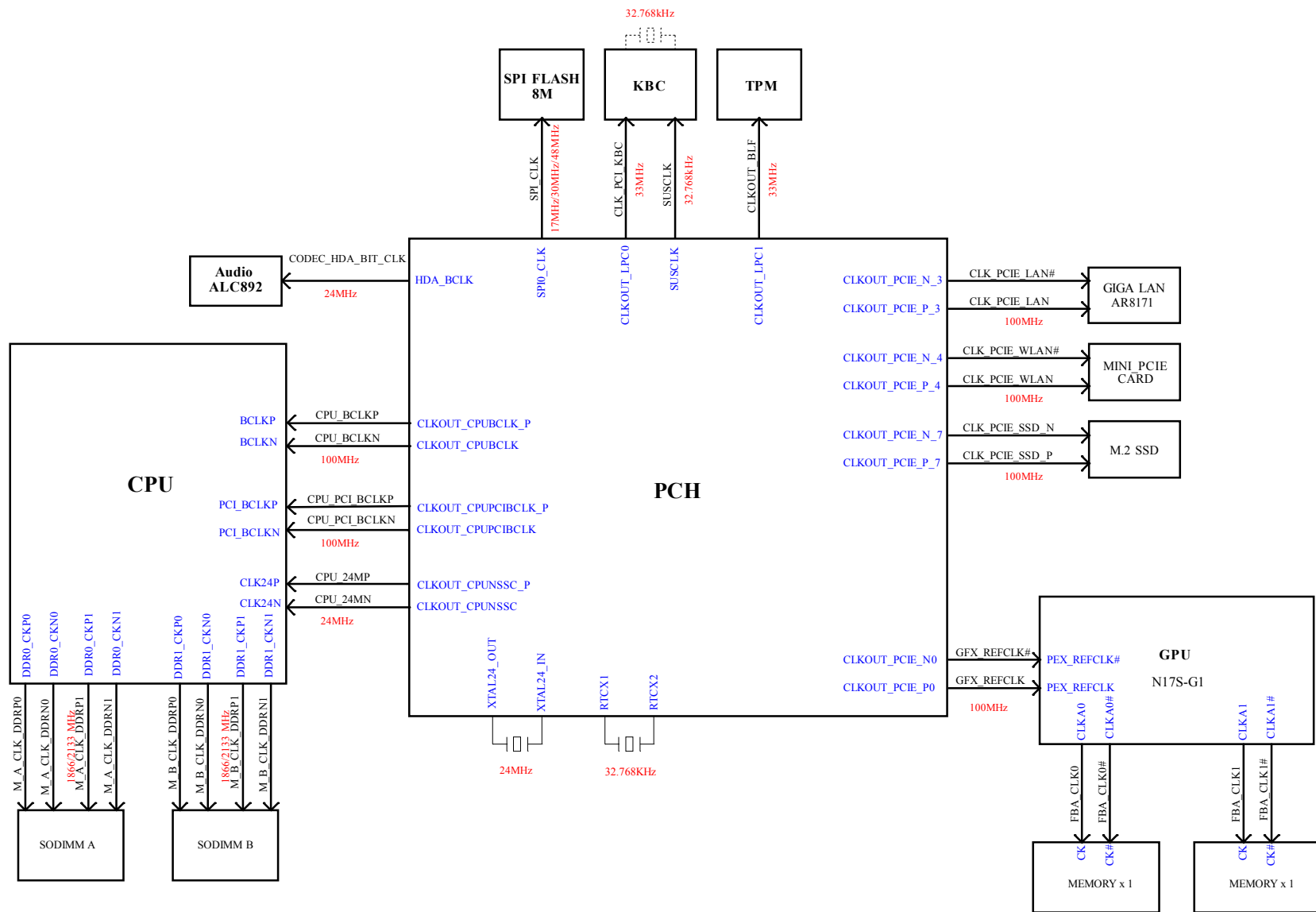


# MS-16JD/MS-179D Intel Kabylake Mobile

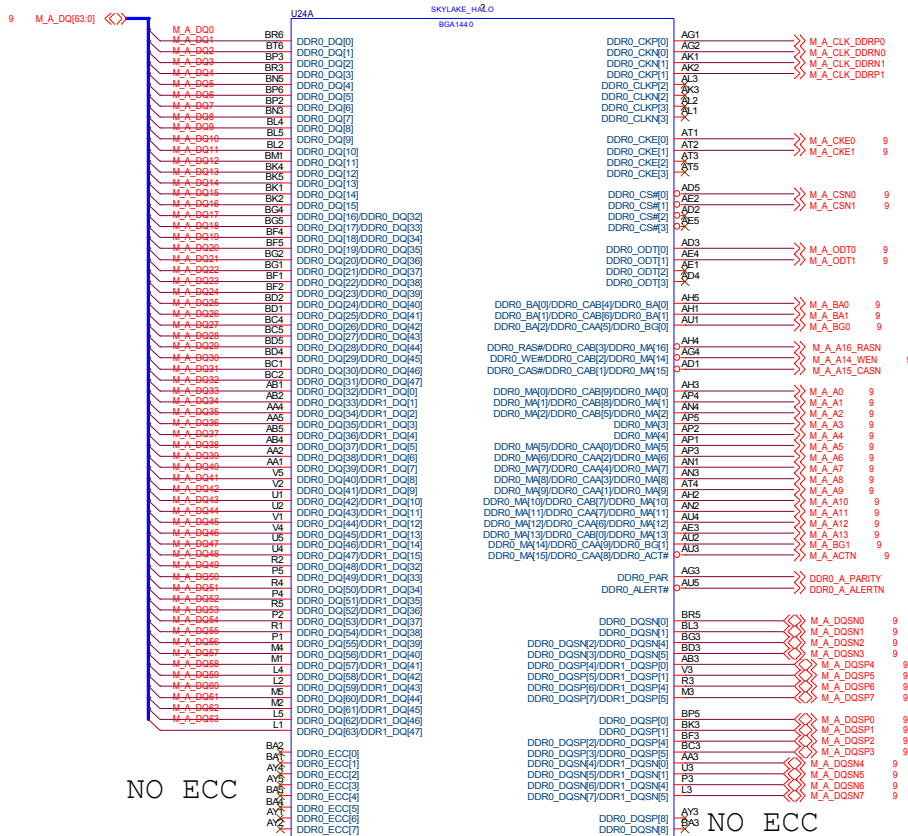
Ver:0A



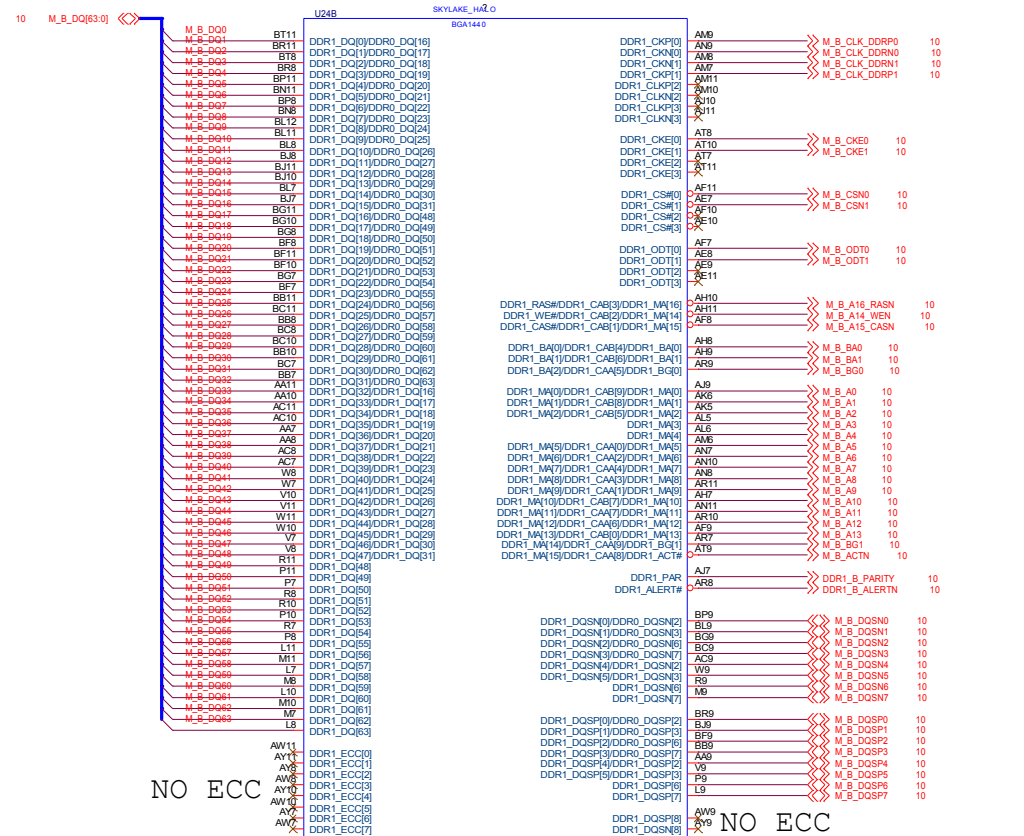




## DDR Channel A



## DDR Channel B

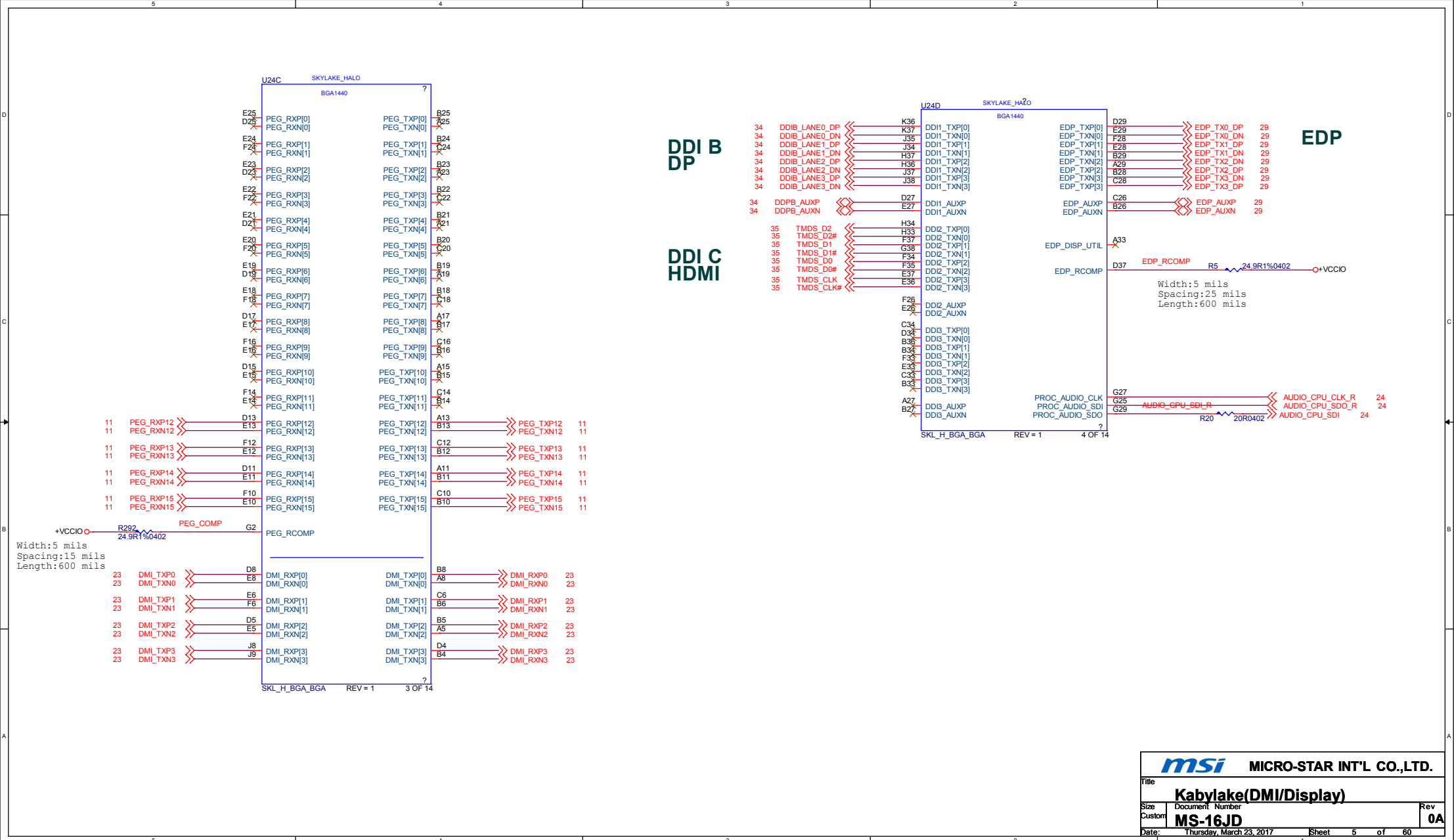


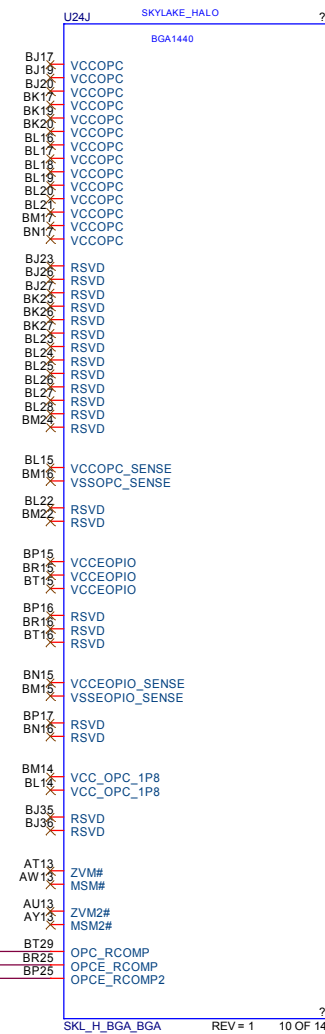
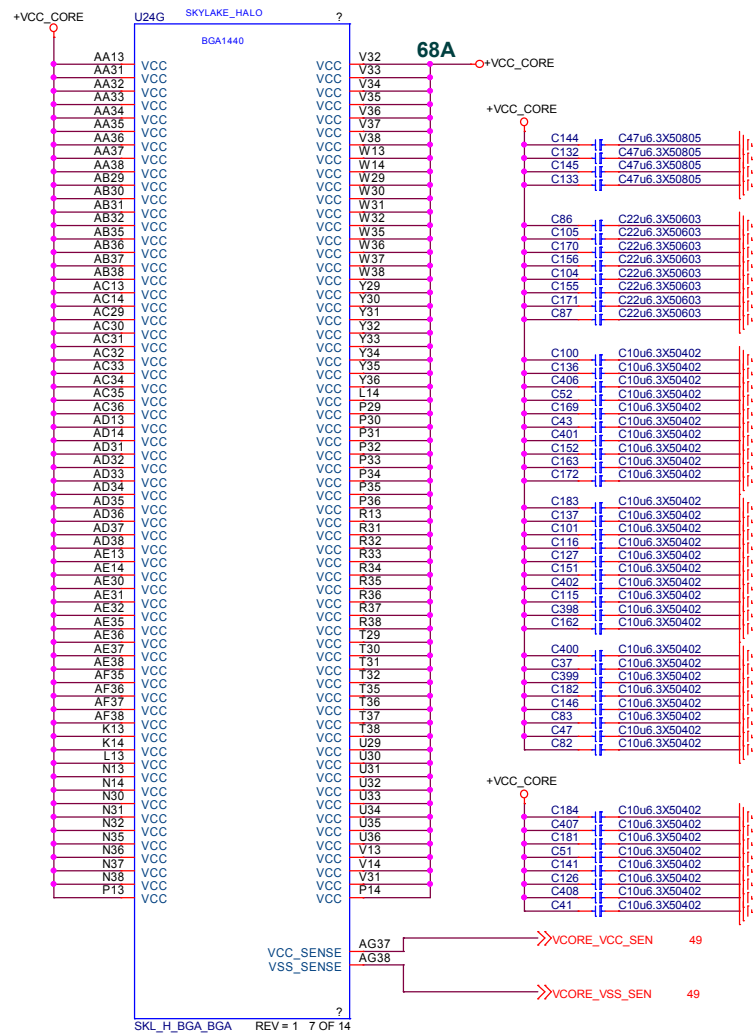
msi MICRO-STAR INT'L CO.,LTD.

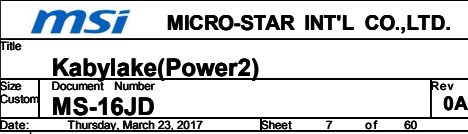
Title **Kabylake(DDR4)**

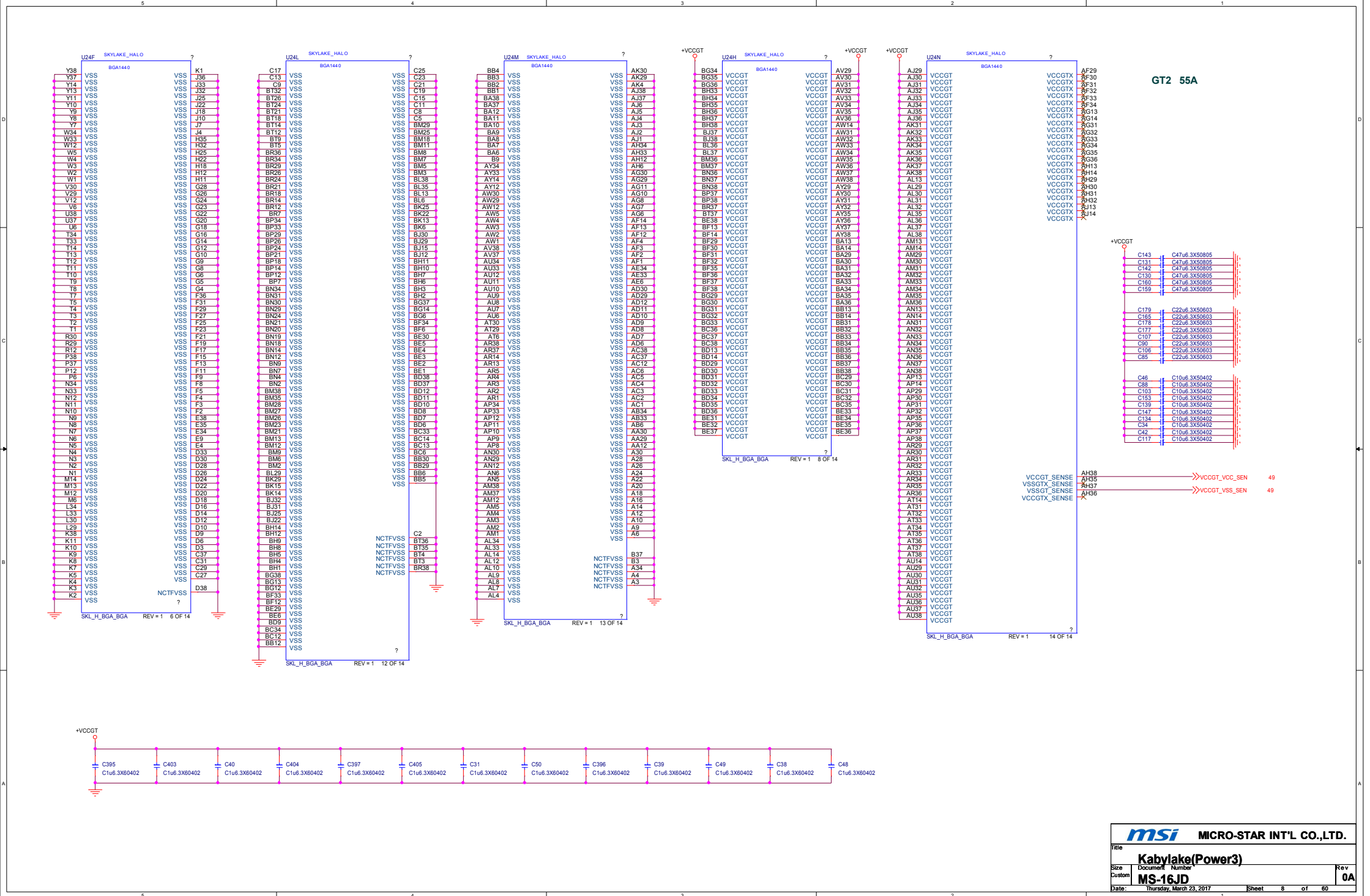
Size	Document	Number	Rev
Custom	<b>MS-16JD</b>		<b>0A</b>

Date: Thursday, March 23, 2017 Sheet 4 of 60

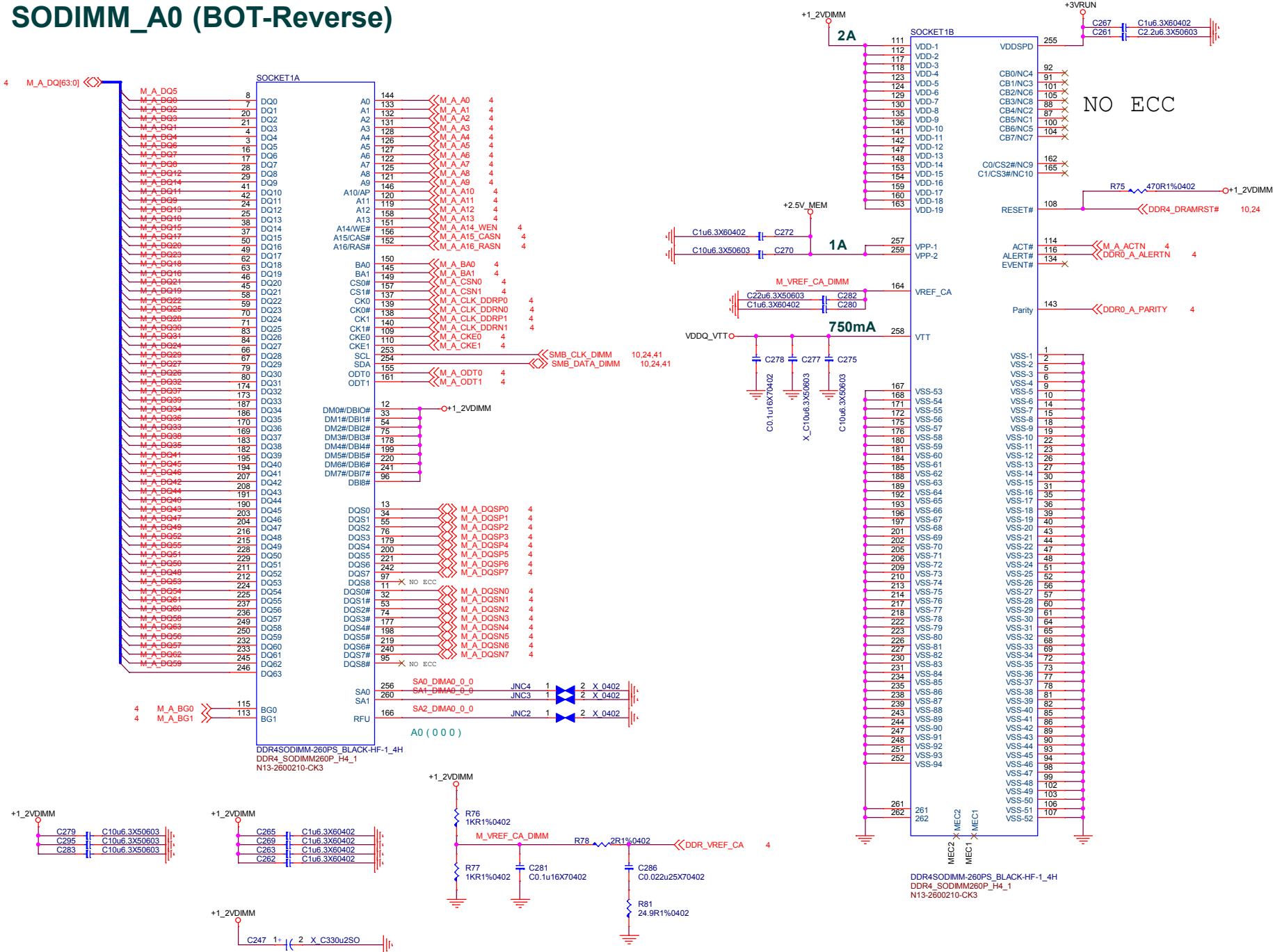




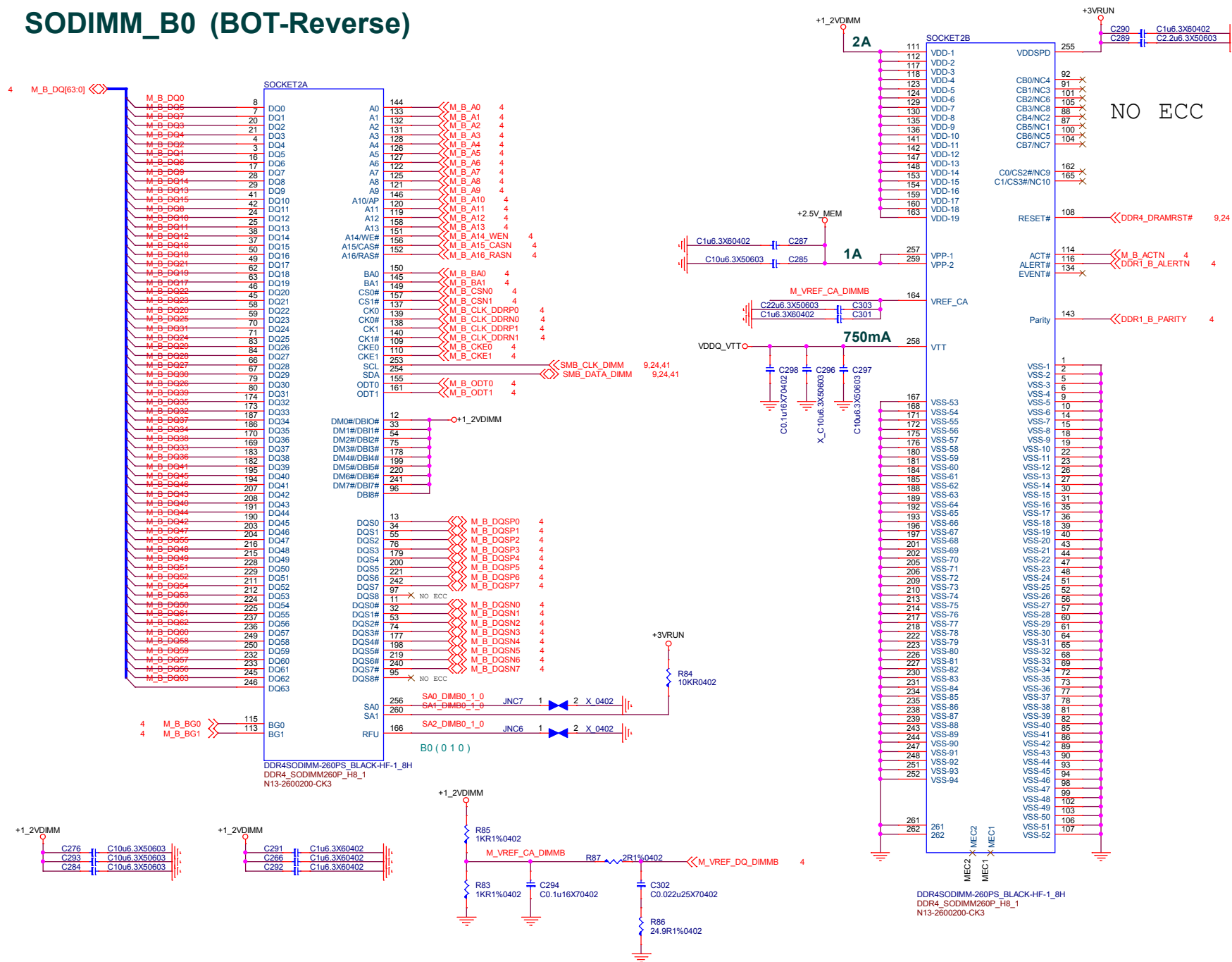




SODIMM\_A0 (BOT-Reverse)



# SODIMM\_B0 (BOT-Reverse)



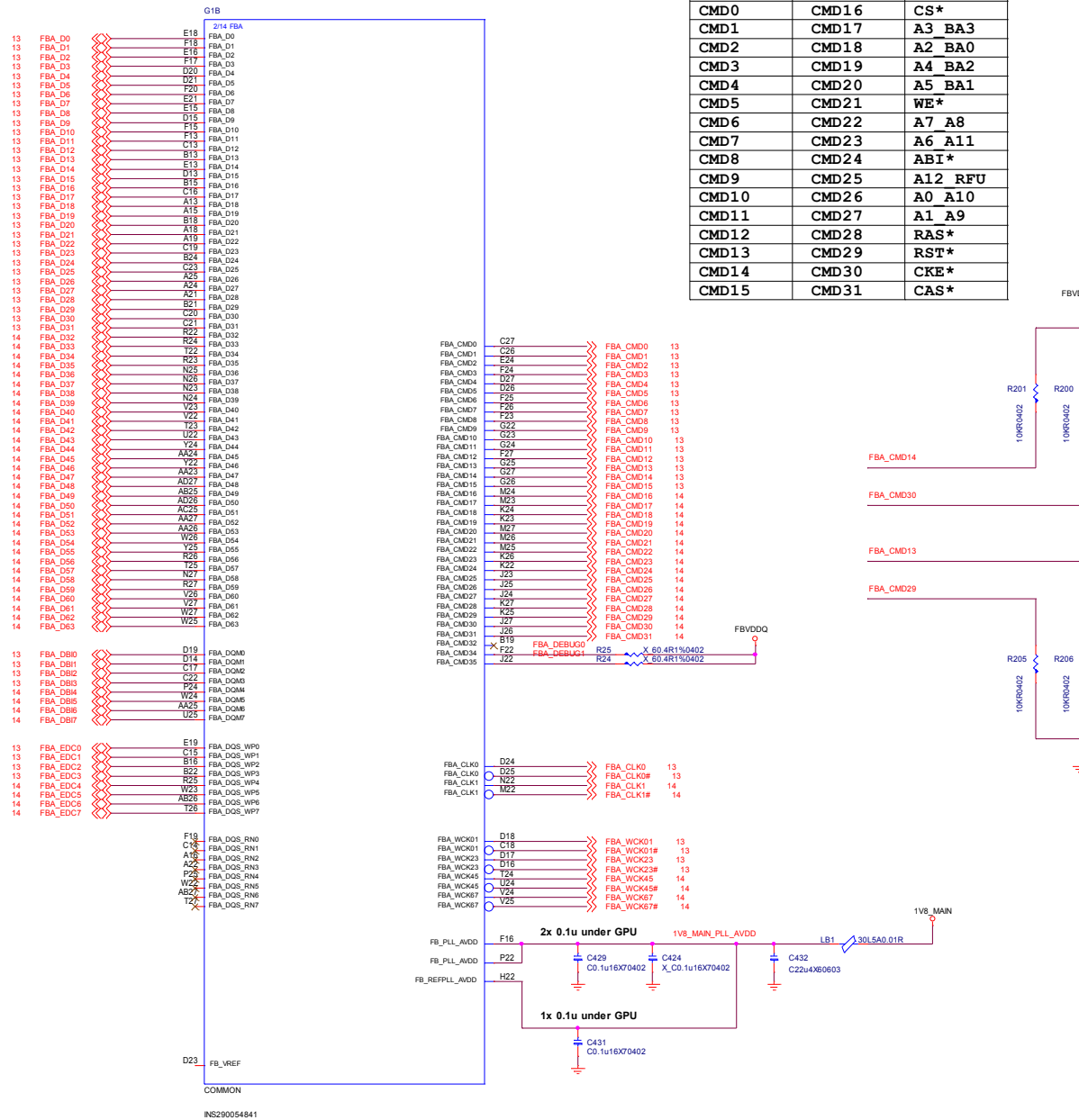
**N17S-G1( PCI-Express Gen3 x4 Interface)**



## N17S-G1( Frame Buffer Interface )

GDD5 Command Mapping GB2C-64

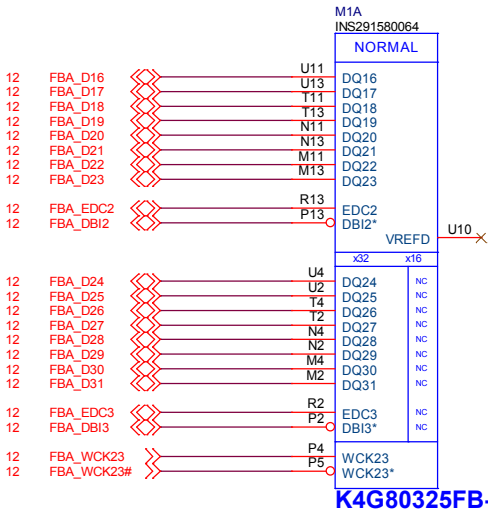
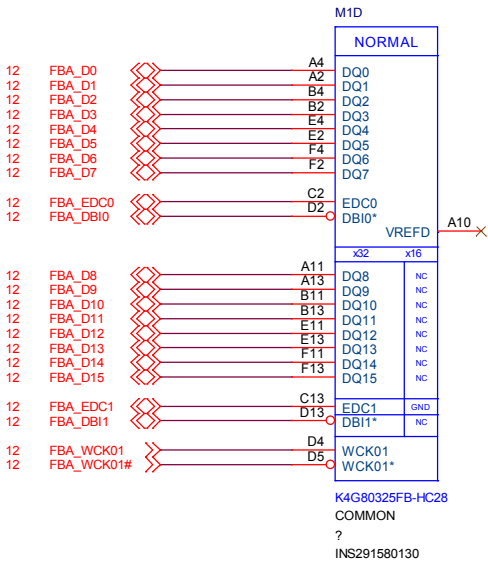
DQ[31:0]	DQ[63:32]	
CMD0	CMD16	CS*
CMD1	CMD17	A3 BA3
CMD2	CMD18	A2 BA0
CMD3	CMD19	A4 BA2
CMD4	CMD20	A5 BA1
CMD5	CMD21	WE*
CMD6	CMD22	A7 A8
CMD7	CMD23	A6 A11
CMD8	CMD24	AB1*
CMD9	CMD25	A12 RFU
CMD10	CMD26	A0 A10
CMD11	CMD27	A1 A9
CMD12	CMD28	RA*
CMD13	CMD29	RST*
CMD14	CMD30	CKE*
CMD15	CMD31	CS*



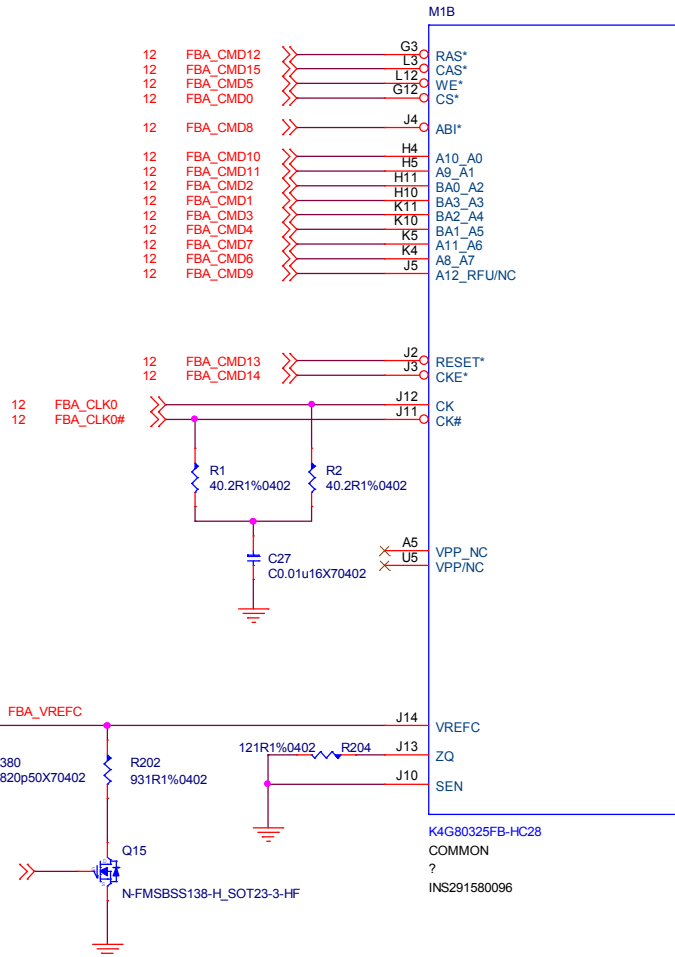
N17S-G1\_GDDR5 Frame A-1

GDD5 Command Mapping GB2C-64

DQ[31:0]		DQ[63:32]	
CMD0	CMD16	CS*	
CMD1	CMD17	A3 BA3	
CMD2	CMD18	A2 BA0	
CMD3	CMD19	A4 BA2	
CMD4	CMD20	A5 BA1	
CMD5	CMD21	WE*	
CMD6	CMD22	A7 A8	
CMD7	CMD23	A6 A11	
CMD8	CMD24	ABI*	
CMD9	CMD25	A12 RFU	
CMD10	CMD26	A0 A10	
CMD11	CMD27	A1 A9	
CMD12	CMD28	RAS*	
CMD13	CMD29	RST*	
CMD14	CMD30	CKE*	
CMD15	CMD31	CAS*	

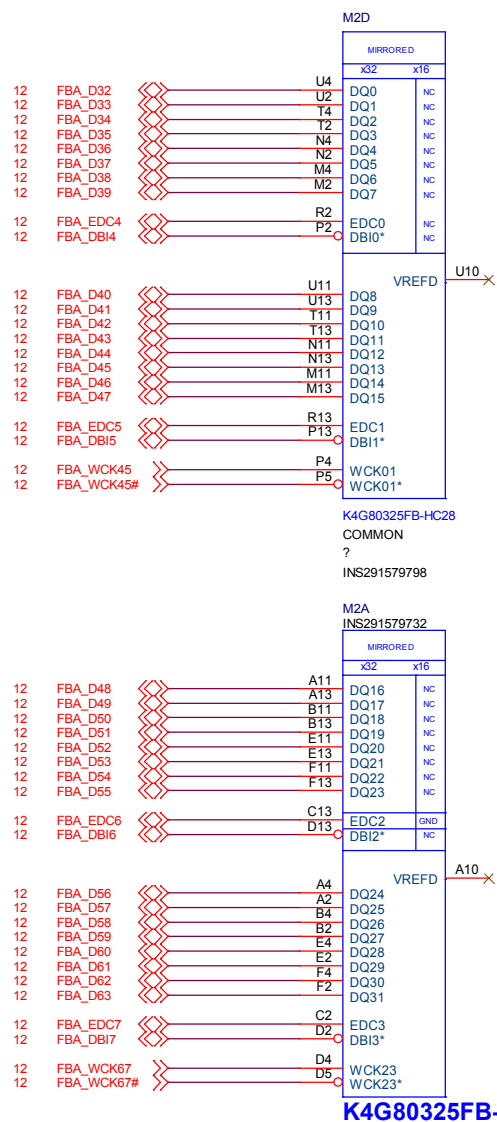


K4G80325FB-HC28



Title			
N17S-G1_GDDR5 Frame A-1			
Size	Document	Number	Rev
B			0A
Date:	MS-1000 23, 2017		
Sheet		13	of 60

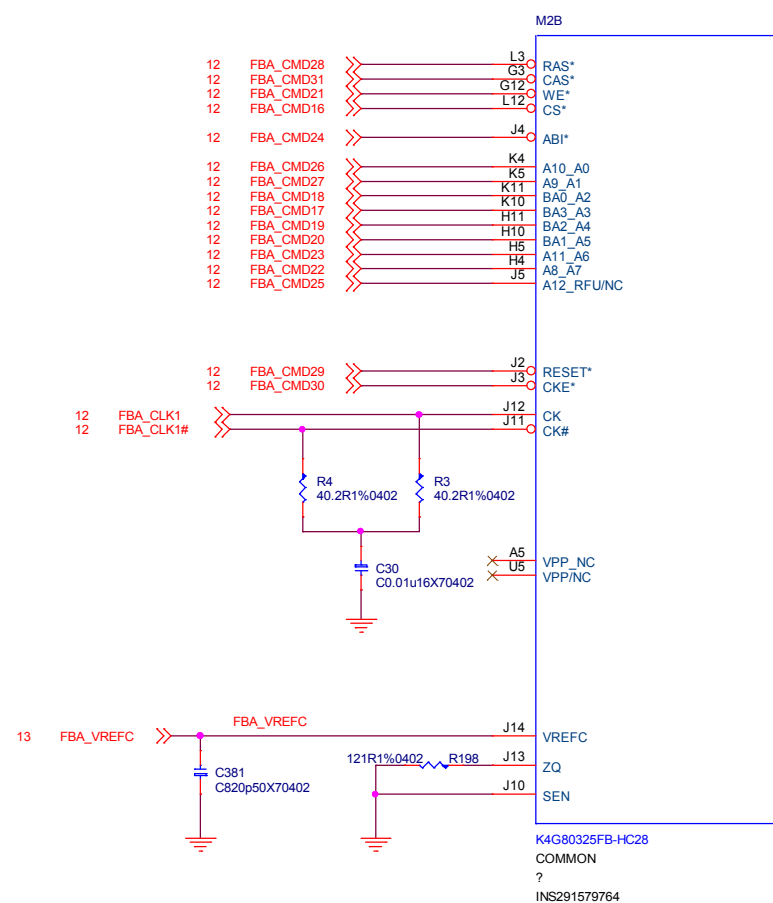
**N17S-G1\_GDDR5 Frame A-2**



**K4G80325FB-HC28**

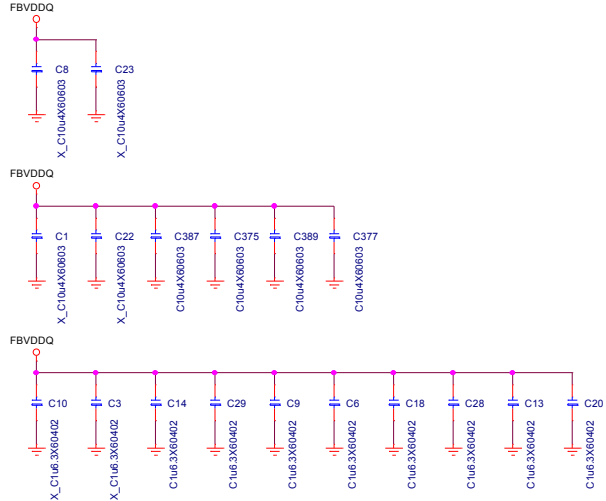
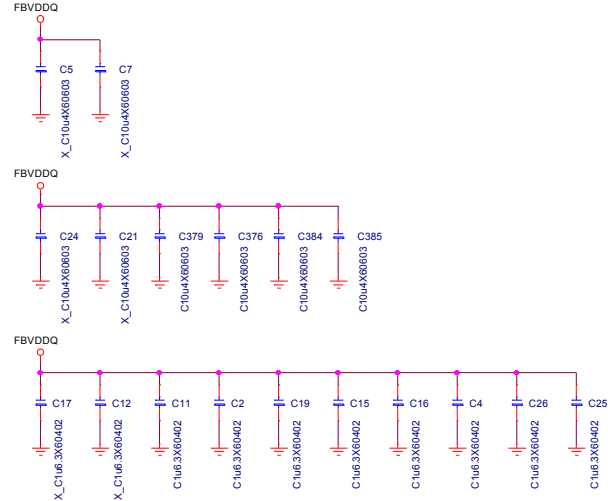
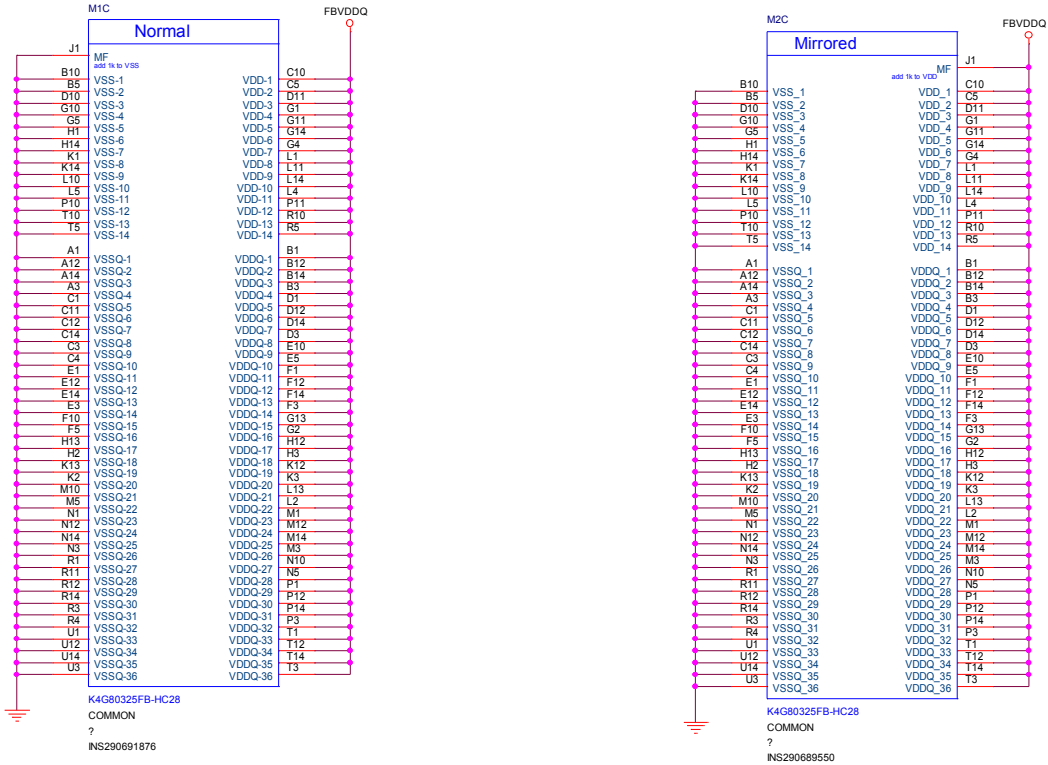
## GDD5 Command Mapping GB2C-64

DQ[31:0]	DQ[63:32]	
CMD0	CMD16	CS*
CMD1	CMD17	A3 BA3
CMD2	CMD18	A2 BA0
CMD3	CMD19	A4 BA2
CMD4	CMD20	A5 BA1
CMD5	CMD21	WE*
CMD6	CMD22	A7 A8
CMD7	CMD23	A6 A11
CMD8	CMD24	ABI*
CMD9	CMD25	A12 RFU
CMD10	CMD26	A0 A10
CMD11	CMD27	A1 A9
CMD12	CMD28	RAS*
CMD13	CMD29	RST*
CMD14	CMD30	CKE*
CMD15	CMD31	CAS*

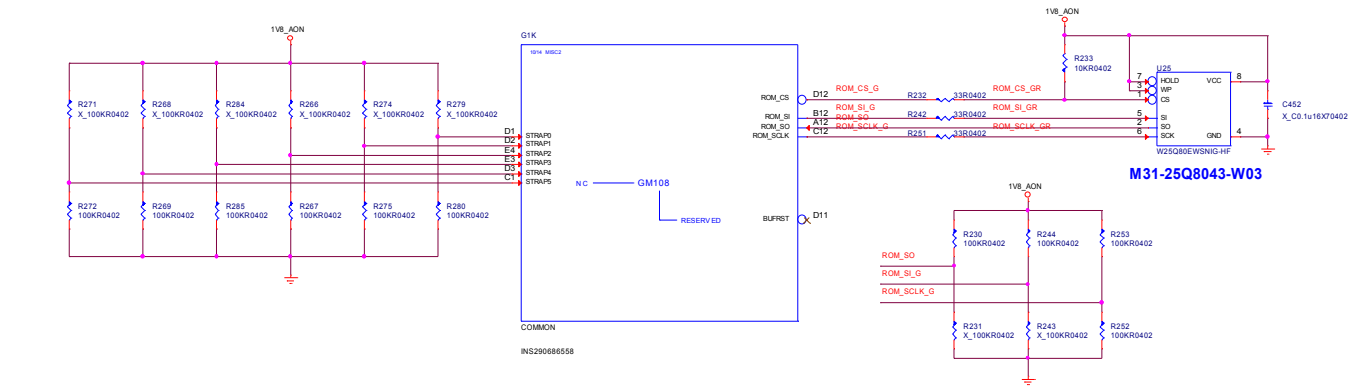


Title			
<b>N17S-G1 GDDR5 Frame A-2</b>			
Size B	Document Number	Rev 0A	
Date:	MC 1618	23, 2017	Sheet 14 of 60

N17S-G1\_GDDR5\_DECOUPLING



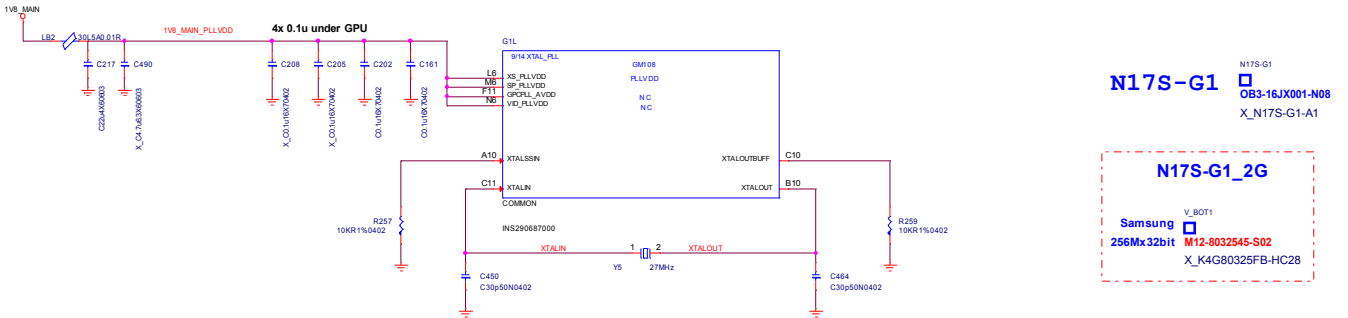
N17S-G1\_VBIOS & Straps



ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED3	SOR_EXPOSED2	SOR_EXPOSED1	SOR_EXPOSED0
L	L	L	1:ENABLE	1:ENABLE	1:ENABLE	1:ENABLE
L	L	H	1:ENABLE	1:ENABLE	0:DISABLE	1:ENABLE
L	H	L	1:ENABLE	1:ENABLE	0:DISABLE	1:ENABLE
L	H	H	1:ENABLE	1:ENABLE	0:DISABLE	0:DISABLE
H	H	H	1:ENABLE	0:DISABLE	0:DISABLE	0:DISABLE
H	H	M	0:DISABLE	0:DISABLE	0:DISABLE	0:DISABLE

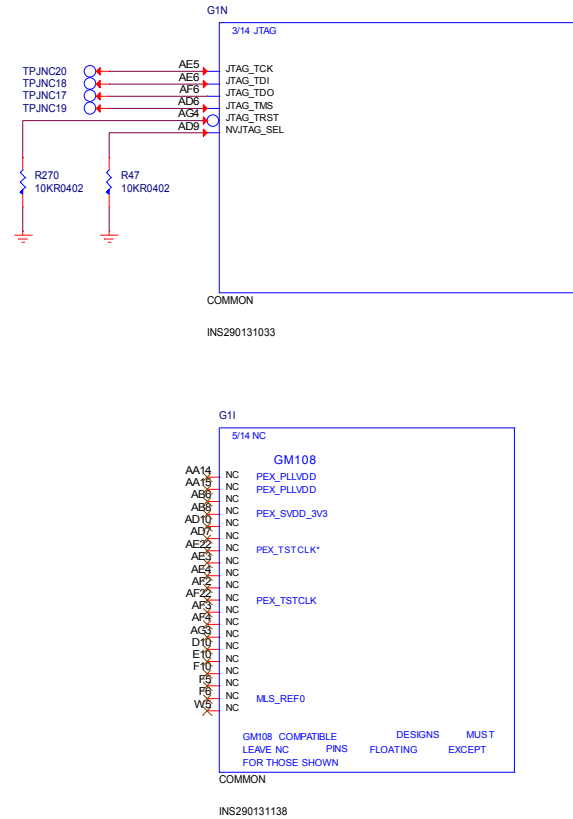
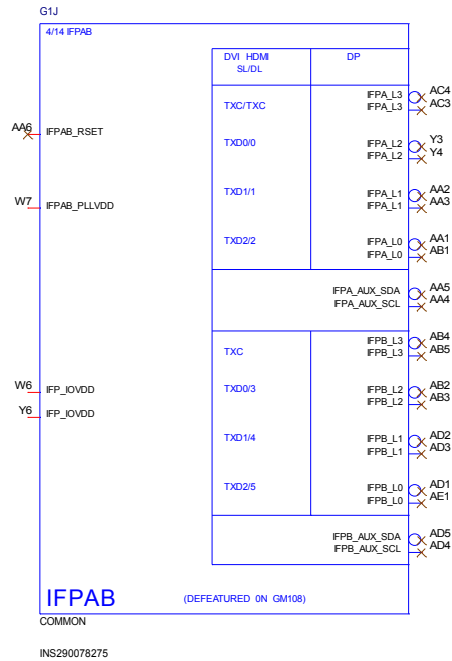
STRAP 5	STRAP 4	STRAP 3	
L	L	L	Optimus
L	L	H	Discrete
H	L	H	Discrete with Gsync

STRAP 2	STRAP 1	STRAP 0			
L	L	L	0x0	Samsung K4G80325FB-HC28	
L	L	H	0x1	Microm M151J2256M32HF-70:A	256M*32
L	H	L	0x2	Hynix H5GC8H24MJR-R0C	
H	H	L	0x6	Hynix H5GC4H24AJR-R0C	
H	H	H	0x7	Samsung K4G41325FE-HC28	128M*32
L	L	M	0x8	Microm EDW40325BAG-70-F	

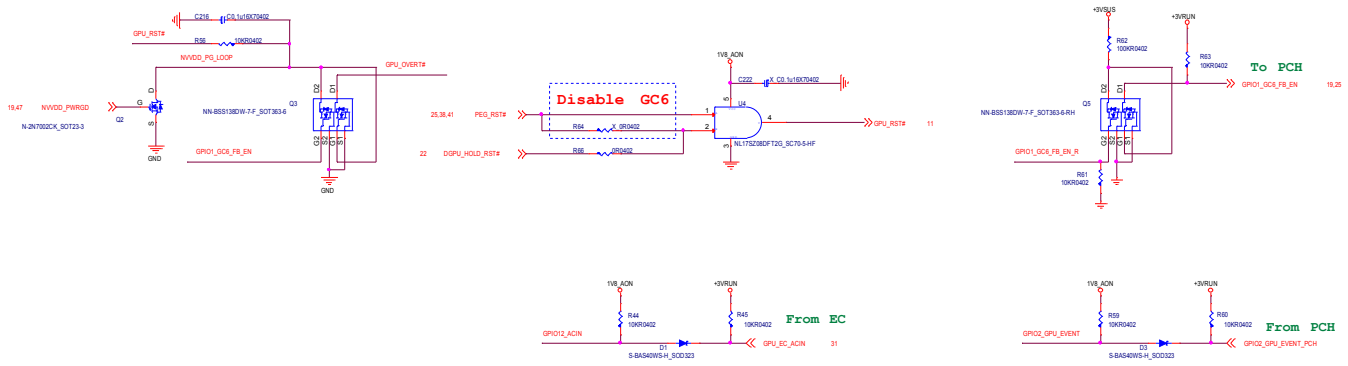
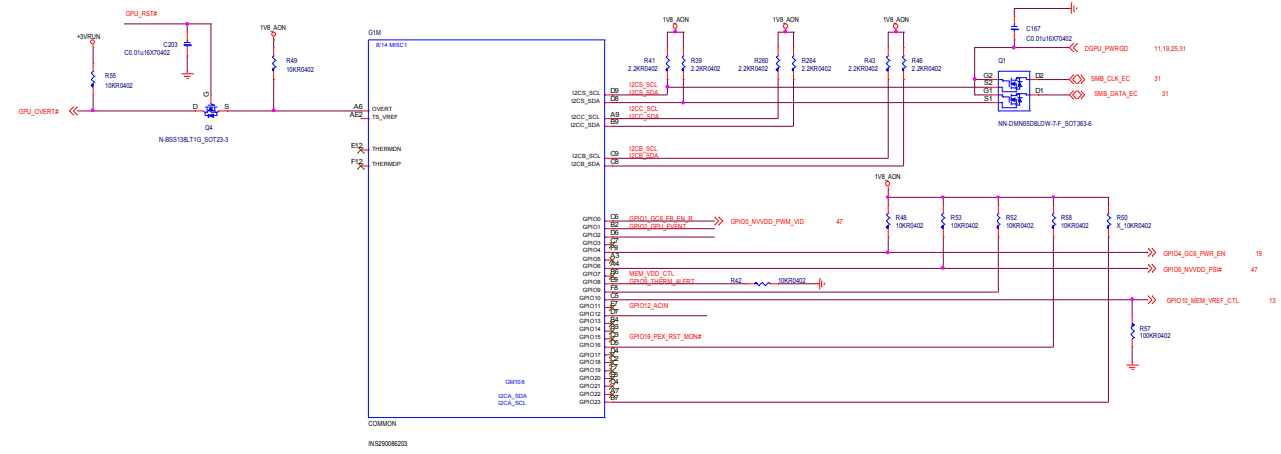


File	Document Number	Rev
N17S-G1_VBIOS & Straps		0A
Date:	MS-1610	Sheet 16 of 60

## N17S-G1\_Display IF



N17S-G1\_GPIO



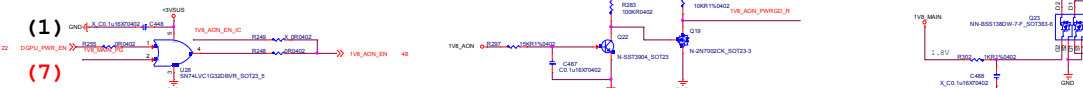
Pin Name	Normal function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	NVVDD_PWM	O	PWM Output To Control NVVDD	0 TO 1V8 PWM Output
GPIO1	GC6M:GC6_FB_EN	O	FB Enable For GC6 2.1	Open Source 10K Pull-Down
GPIO2	GC6M:GC6_EVENT / WAKE	I	GPU Wake Signal For GC6 2.1	10K Pull-Up To 1V8 AON Unless Driven Actively
GPIO3	NVVDD_PWM(NC)	I/O	PWM Output To Control The NVVDD Power Supply	0 TO 1V8 Output
GPIO4	GC6M:1V8_MAIN_EN	O	GPU Power Sequencing For GC6 2.1	Open Drain 10K Pull-Up To 1V8 AON
GPIO5	FRM_LCK(NC)	I	Active Low Frame Lock	Open Drain 10K Pull-Up To 1V8 AON
GPIO6	NVVDD_PSI/NVVDD_PSI	O	Phase Shedding	10K Pull-Up To 1V8 AON To Enable Multiple Phases
GPIO7	LCD_BL_PWM(NC)	O	Panel Backlight Enable	100K pull-down
GPIO8	MEM_VDD_CTL	O	Memory Voltage Control	Pull-Up/Pull-Down To Set The FBVDD/Q Power ON Voltage
GPIO9	THERM_ALERT	I/O	Active Low Thermal Alert	Open Drain 10K Pull-Up To 1V8 AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100K pull-down
GPIO11	LCD_VDD	O	Panel Power Enable	100K pull-down
GPIO12	PWR_LEVEL	I	AC Power Detect Or Power Supply Overdraw Input	100K Pull-Up To 1V8 AON
GPIO13	LCD_BLEN(NC)	O	LCD Panel Backlight Enable	Panel Backlight Enable
GPIO14	HFD_IPFA	I	Hot Plug Detect for IPFA	
GPIO15	HFD_IPFB	I	Hot Plug Detect for IPFB	
GPIO16	GC6M:SYS_PEX_RST_MON	I	System Side PCIe Reset Monitor	10K Pull-Up To 1V8 AON Unless Driven Actively
GPIO17	UNUSED(NC)	I/O		
GPIO18	UNUSED(NC)	I/O		
GPIO19	3D_Vision(NC)	O	3D Vision L/R signal	100K pull-down
GPIO20	GC5_MODE(NC)	I/O		
GPIO21	MEM_VDD_CTL(NC)	O	Frame Buffer VDD Select	Open Drain Pull-Up/Pull-Down To Set The FBVDD/Q Power ON Voltage At Boot Up
GPIO22	UNUSED(NC)	I/O		
GPIO23	GC6M:GPU_PEX_RST_HOLD	O	GPU PCIe Self Reset Control	Open Drain 10K Pull-Up To Gated 3V3

## N175-G1\_Power Control

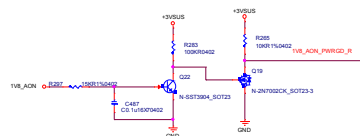
Power on = 1V8\_AON -> 1V8\_MAIN -> NVVDD+NVVDDS -> PEX\_VDD -> FBVDDQ -> DGPUPWRGD

Power down = PEX\_VDD/FBVDDQ -> NVVDD+NVVDDS -> 1V8\_MAIN -> 1V8\_AON

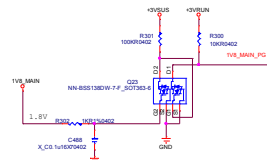
### 1V8\_AON



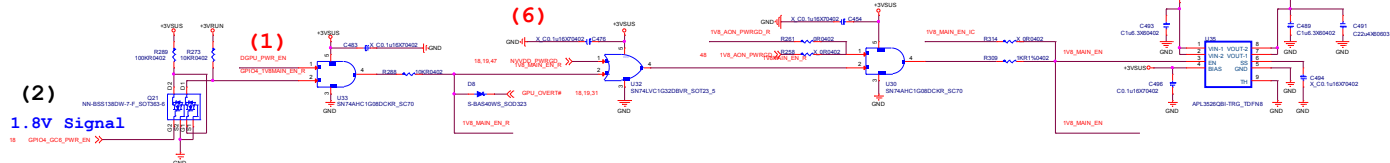
### 1V8\_AON POWER GOOD



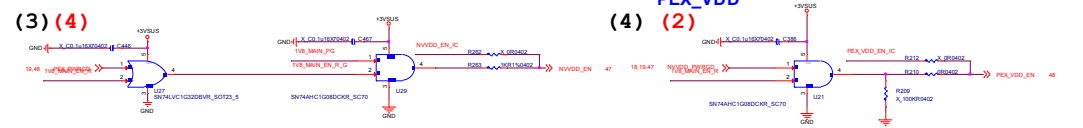
### 1V8\_MAIN POWER GOOD



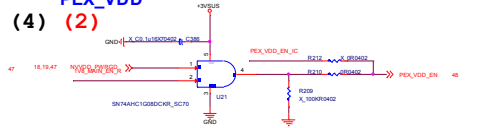
### 1V8\_MAIN



### NVVDD



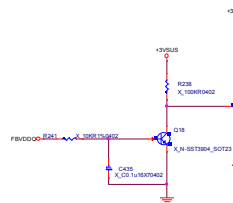
### PEX\_VDD



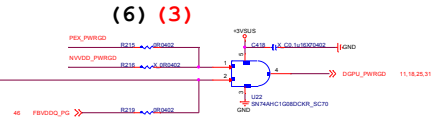
### FBVDDQ



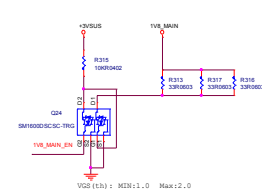
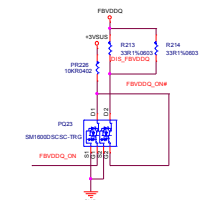
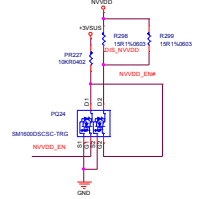
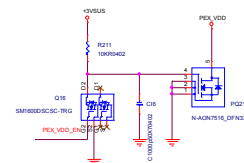
### FBVDDQ POWER GOOD



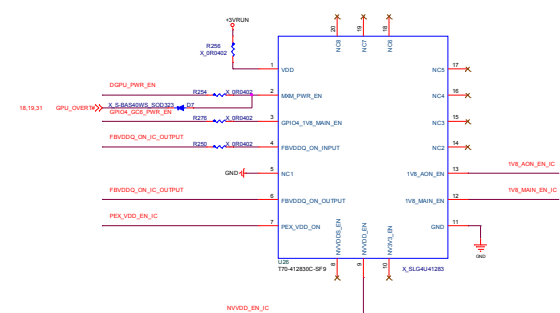
### DGPU POWER GOOD



## Discharge Circuit



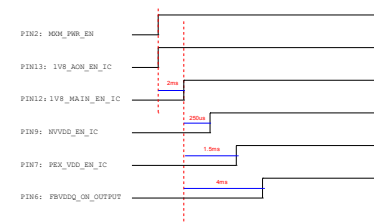
## SLG4U41283 Power Sequence Control IC



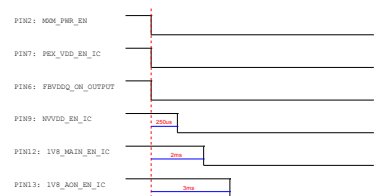
PIN2: MXM\_PWR\_EN is 3.3V  
PIN3: GPIO4\_GC6\_PWR\_EN is 1.8V  
PIN4: FBVDDQ\_ON\_INPUT 3.3V  
PIN6: FBVDDQ\_ON\_OUTPUT 3.3V  
PIN7: PEX\_VDD\_EN\_IC 3.3V  
PIN9: NVVDD\_EN\_IC 3.3V  
PIN12: 1V8\_MAIN\_EN\_IC 3.3V  
PIN13: 1V8\_AON\_EN\_IC 3.3V

INPUT  
INPUT  
INPUT  
OUTPUT  
OUTPUT  
OUTPUT  
OUTPUT  
OUTPUT

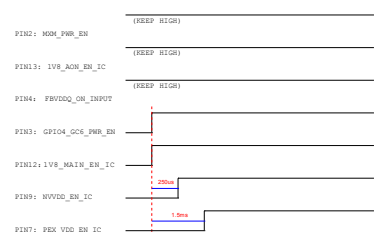
## Power Up Sequence



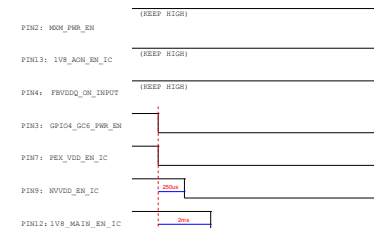
## Power Down Sequence



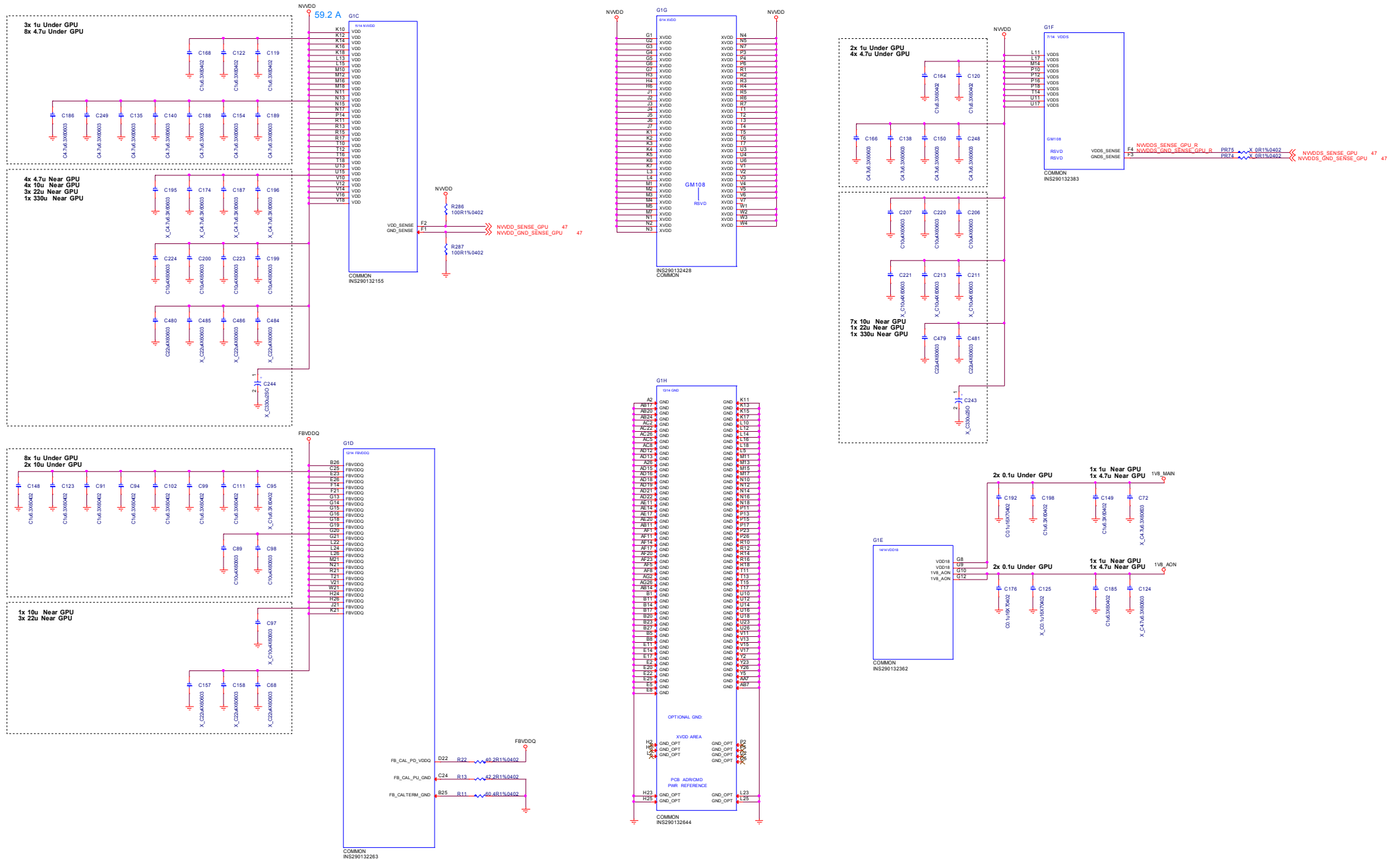
## GC6 2.1 Exit Sequence



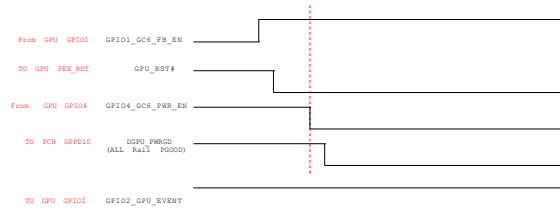
## GC6 2.1 Entry Sequence



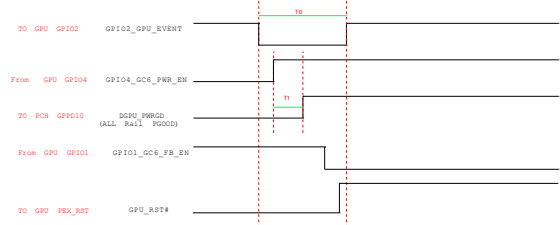
## N17S-G1\_Power & GND



# GC6 2.1 ENTRY SEQUENCE



# GC6 2.1 EXIT SEQUENCE



# GC6 2.1 TIMING

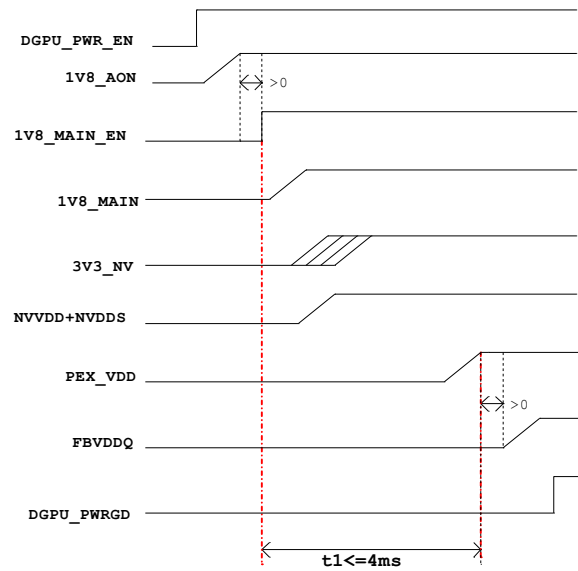
	Min	Max	Unit	Description
T0	0.001	N/A	ms	GPU_EVENT# assertion
T1	0.04	4	ms	3V3_MAIN_EN assertion to all power rails up and stable

# NOTES:

1. ALL RailPGOOD=1 represents all GPU power rails are ramped up and in regulation. If any GPU power rail cannot ge guaranteed in regulation this state should equal to 0.
2. During GC6 exit, the order of power rail ramp-up must follow the Power up sequence described in Chapter 3 with the exception that FBVDD/Q stays on.
3. All delays should be minimized to increase time spent in GC6 for maximum power saving.
4. The entire entry and exit sequence must complete within 200 ms.

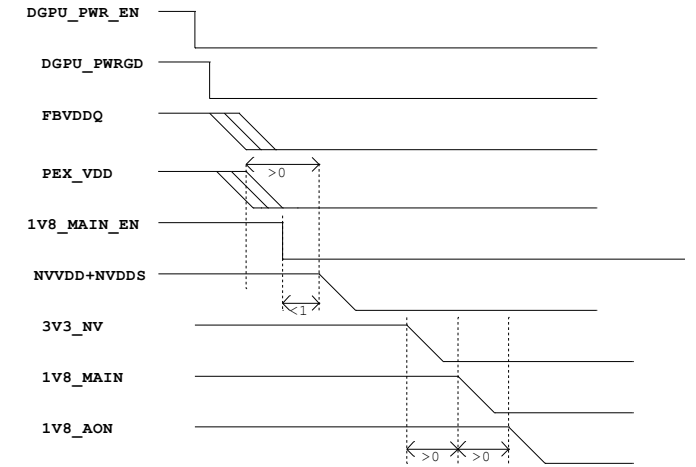
# POWER UP Sequence

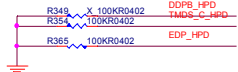
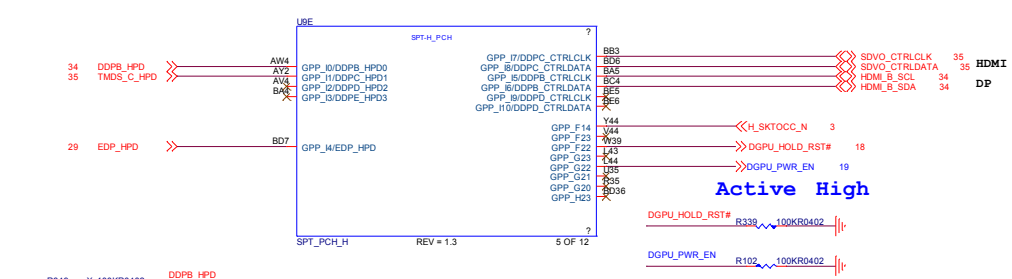
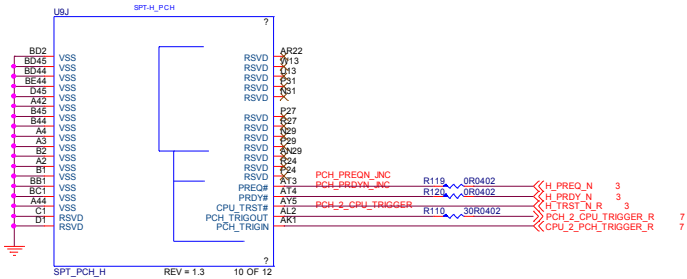
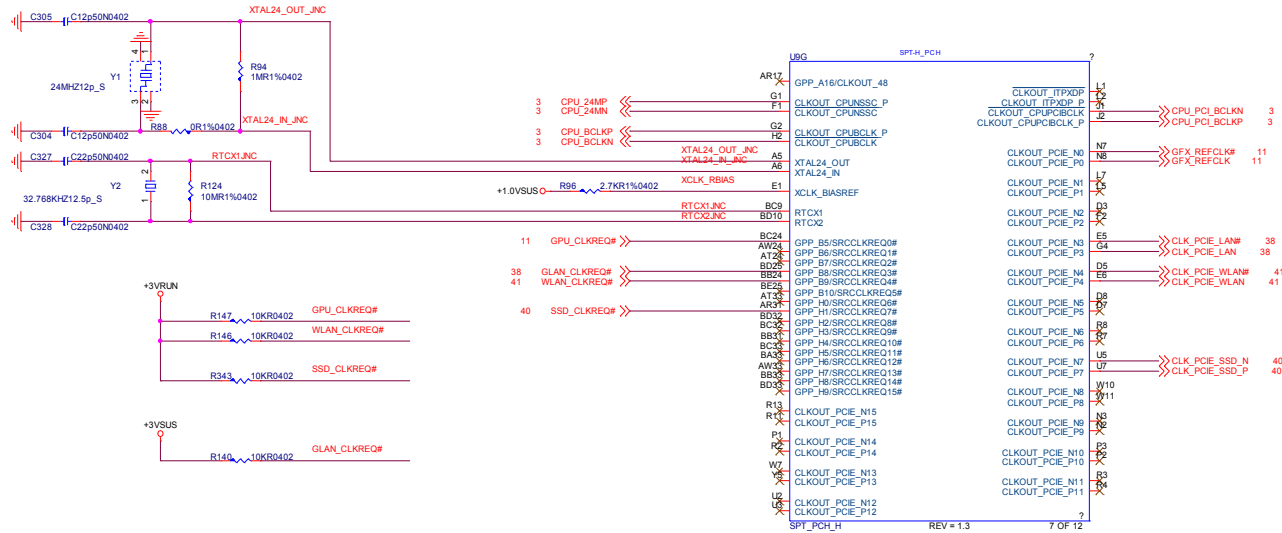
1V8\_AON -> 1V8\_MAIN->NV3V3 -> NVVDD+ NVVDDS / PEX\_VDD -> FBVDDQ



# POWER Down Sequence

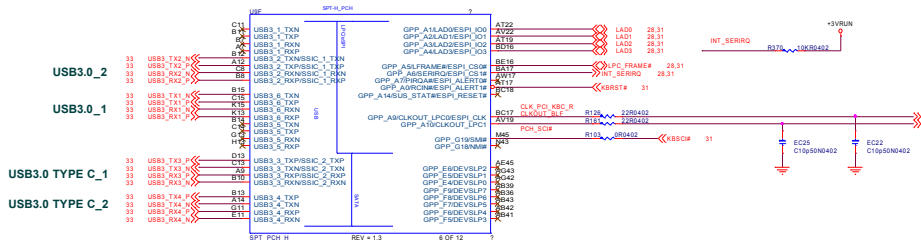
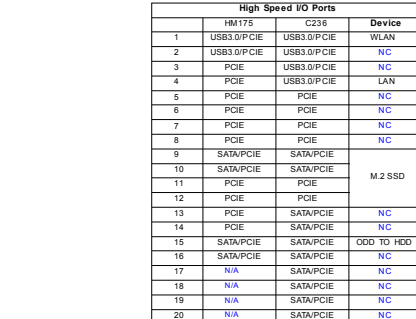
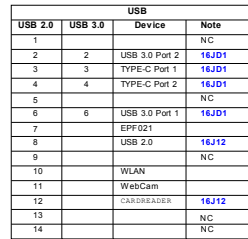
PEX\_VDD/FBVDDQ -> NVVDD+NVVDS -> NV3V3 -> 1V8\_MAIN -> 1V8\_AON

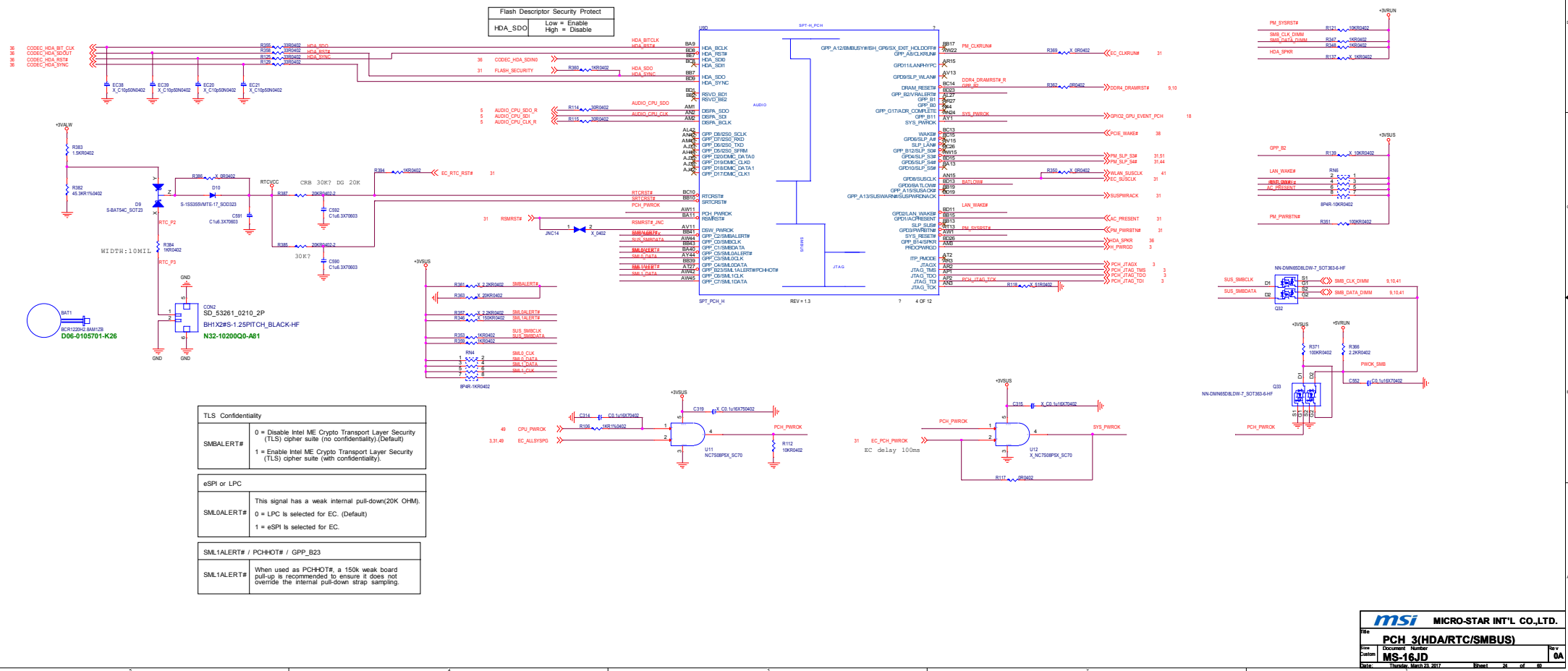




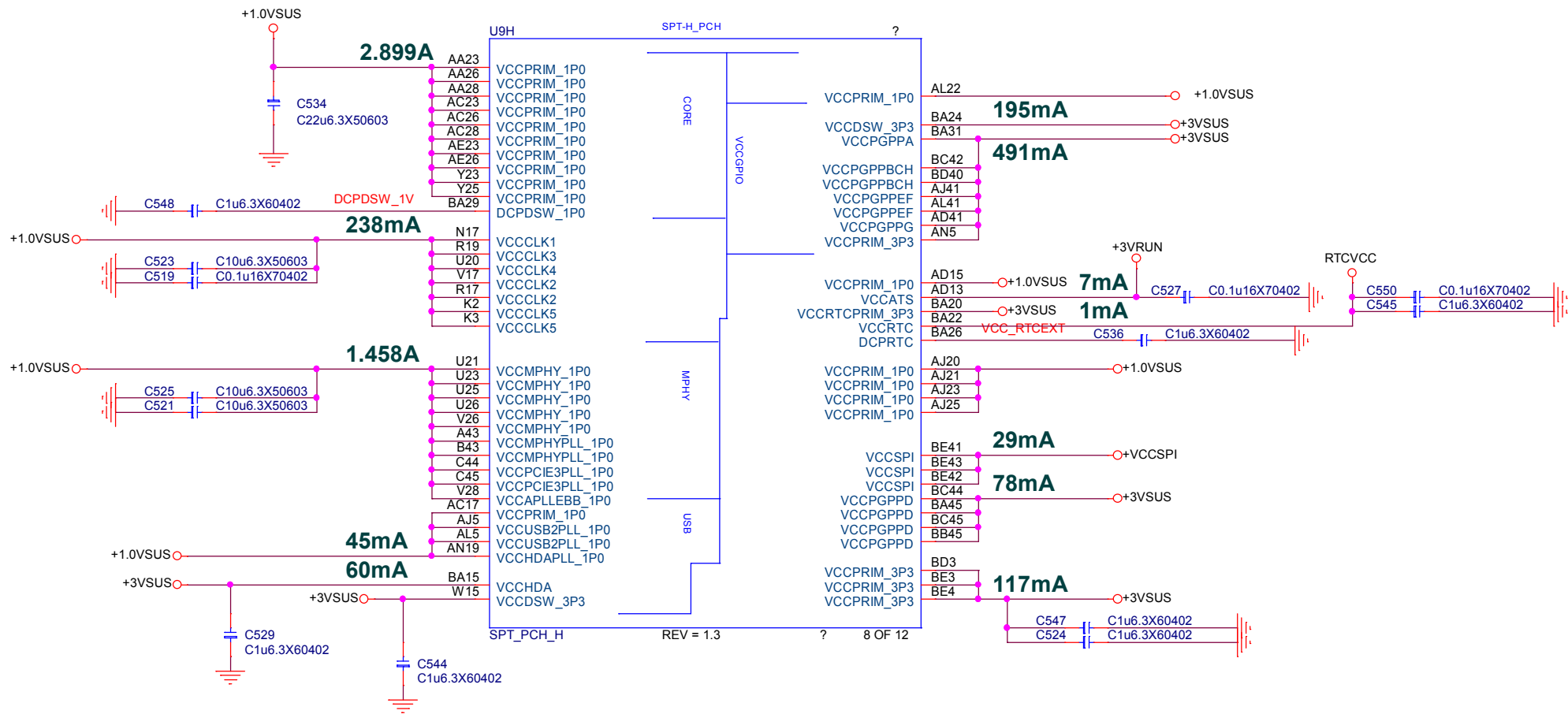
Signal	GPIO Assignment
DGPU_PWR_EN#	GPP_G22
DGPU_PWROK	NA
DGPU_HOLD_RST#	GPP_F22

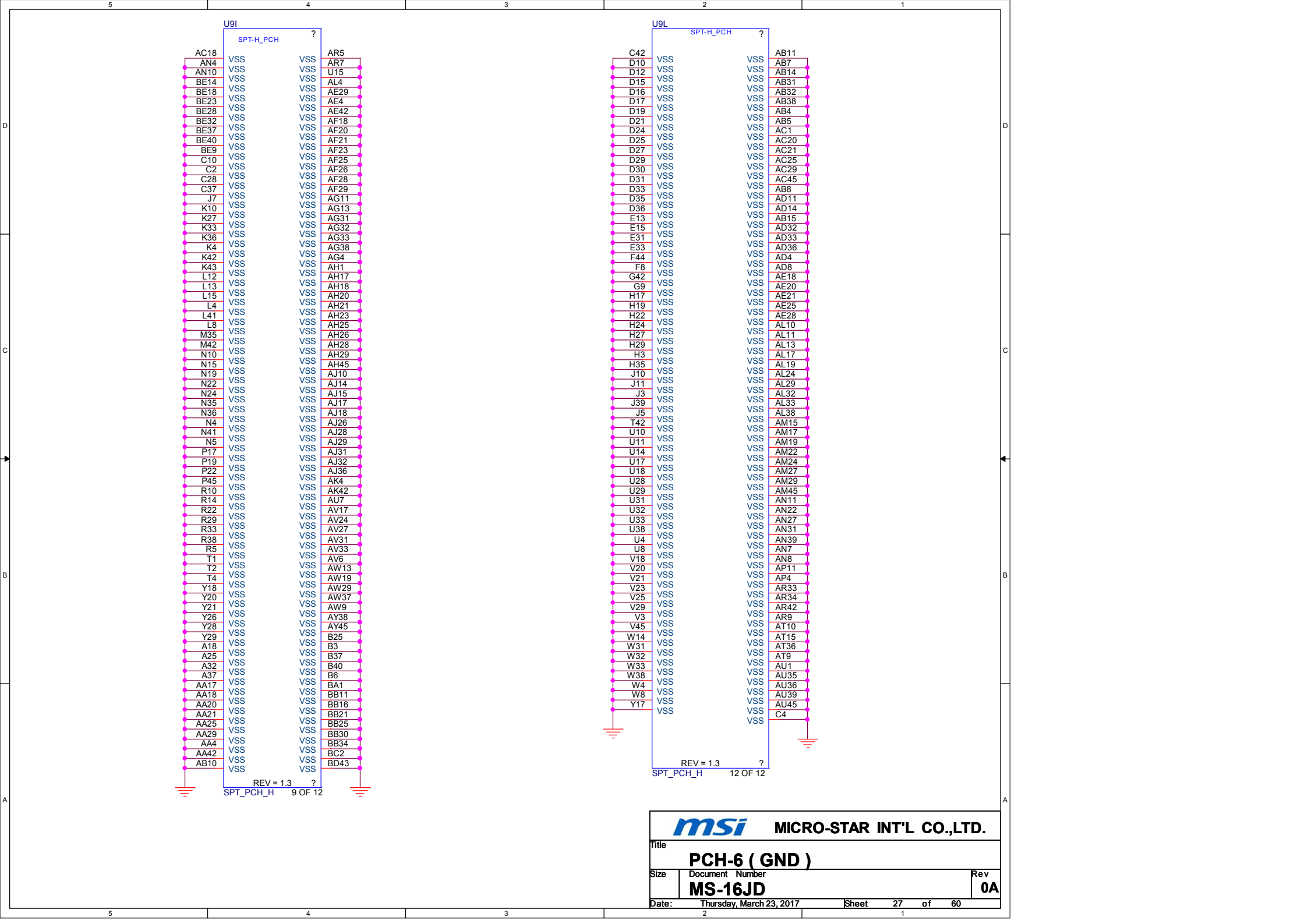
Active High







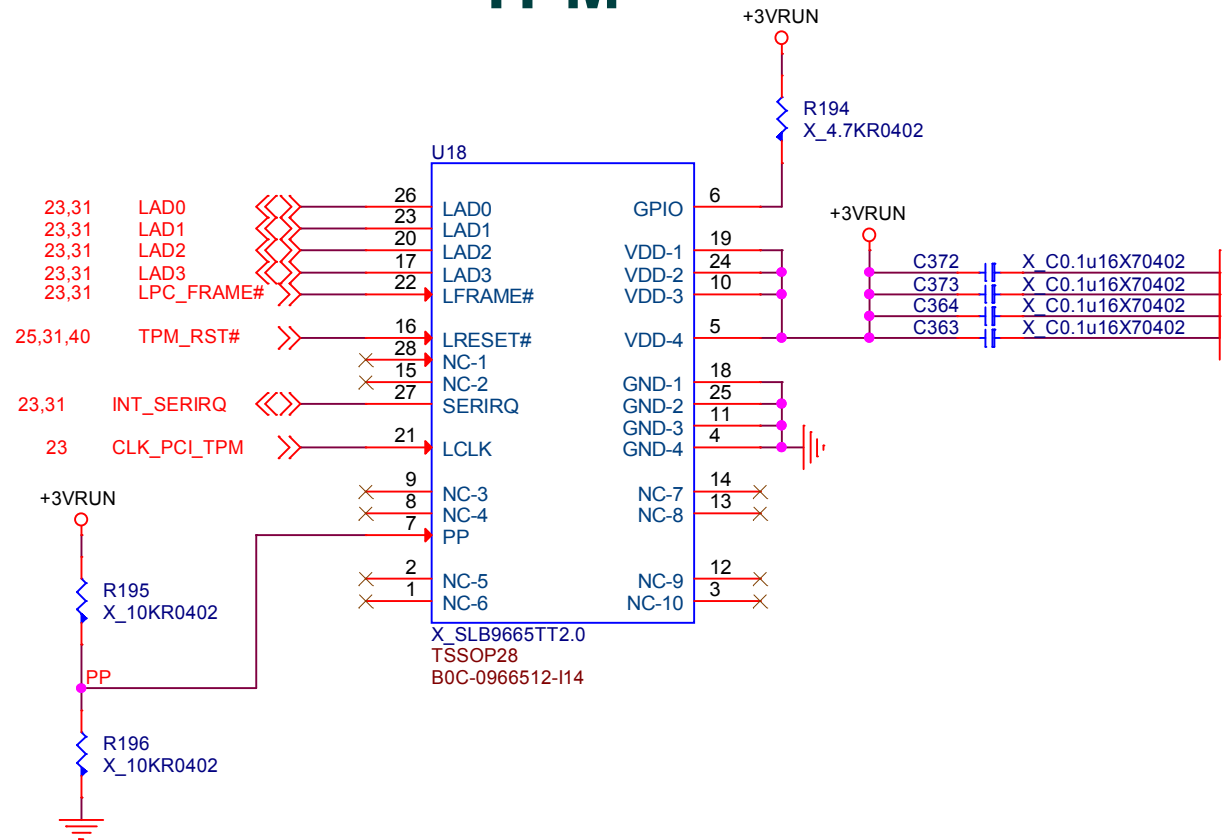




MICRO-STAR INT'L CO.,LTD.

Title		
PCH-6 ( GND )		
Size	Document Number	Rev
MS-16JD		0A
Date:	Thursday, March 23, 2017	Sheet 27 of 60

# TPM



MICRO-STAR INT'L CO.,LTD.

Title

**TPM**

Size

Document Number

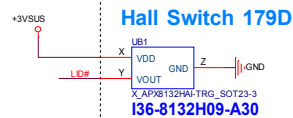
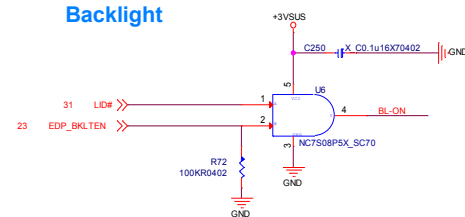
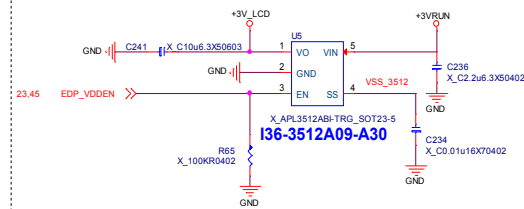
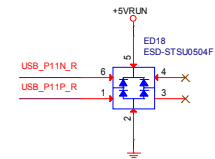
**MS-16JD**

Rev

**0A**

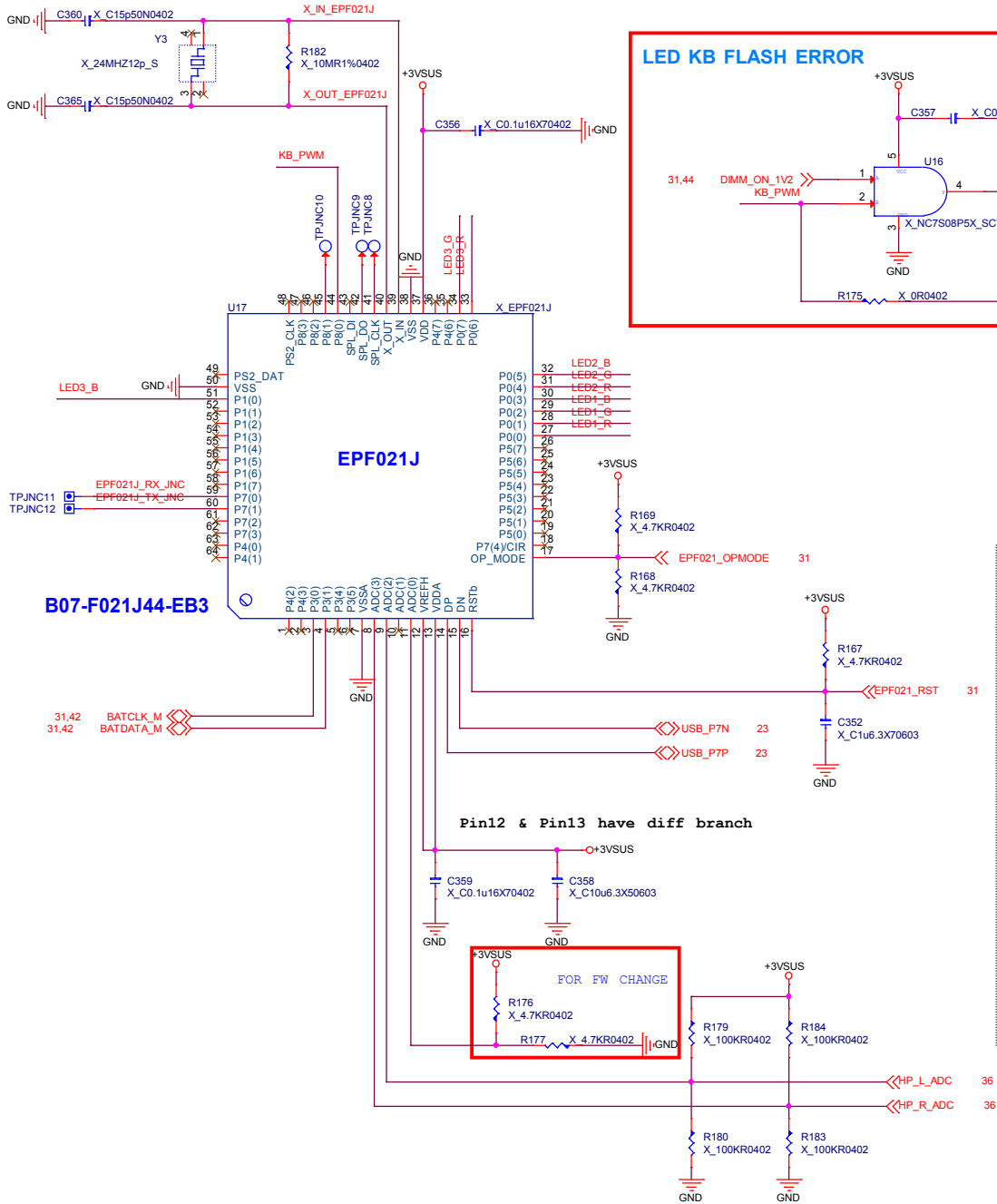
Date: Monday, April 10, 2017

Sheet 28 of 60

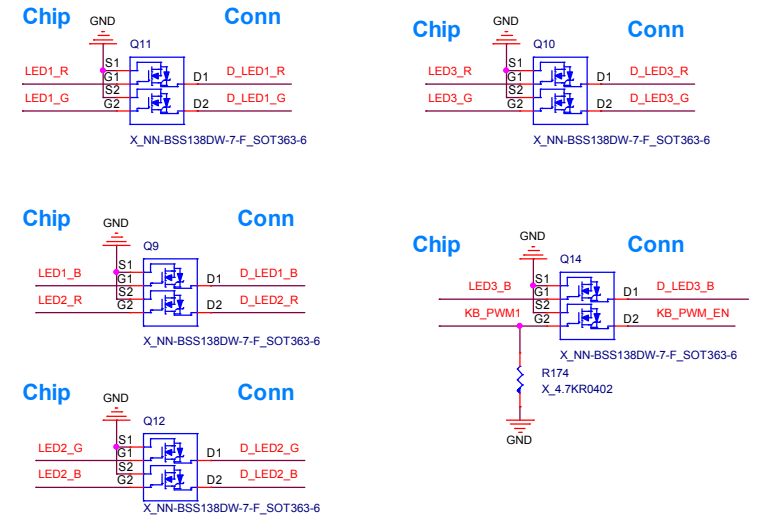


## Keyboard LED (EPF021J)

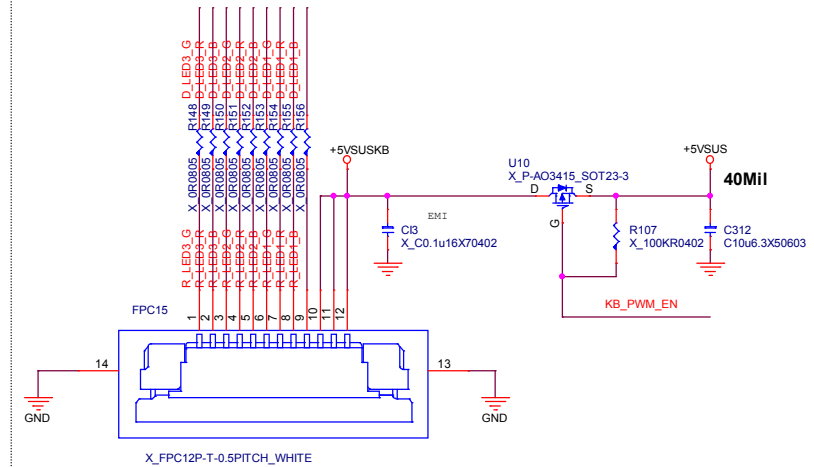
C749 and C750 change to 15pF for SA



EPF021J Sink current not enough, only using BSS138 (0.22A)



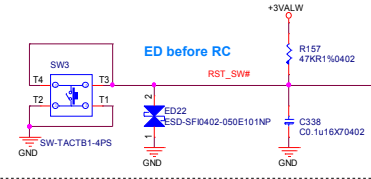
## LED Keyboard CONN



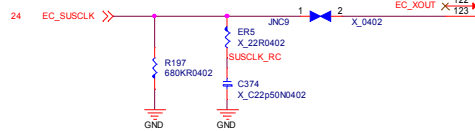
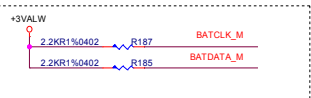
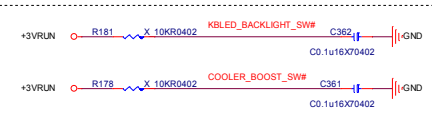
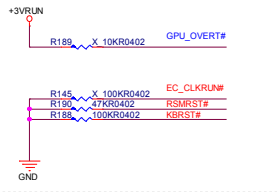
LED Keyboard Pin Define	
Pin 1	VCC_G
Pin 2	VCC_R
Pin 3	VCC_B
Pin 4	LED1_B
Pin 5	LED1_R
Pin 6	LED1_G
Pin 7	LED2_B
Pin 8	LED2_R
Pin 9	LED2_G
Pin 10	LED3_B
Pin 11	LED3_R
Pin 12	LED3_G

## EC (ENE9028)

## Hardware Reset



PU/PD



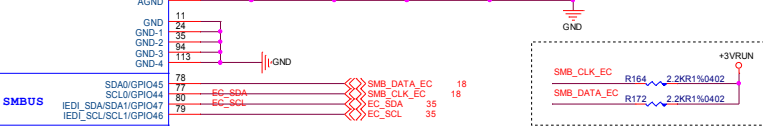
ALLSYSPG



## MB\_



## POWER/GRO



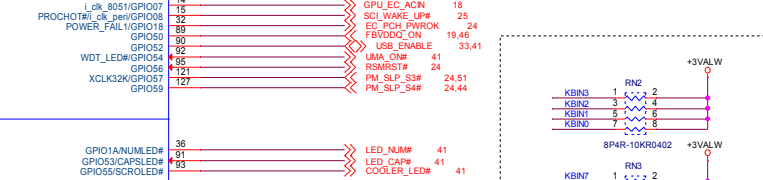
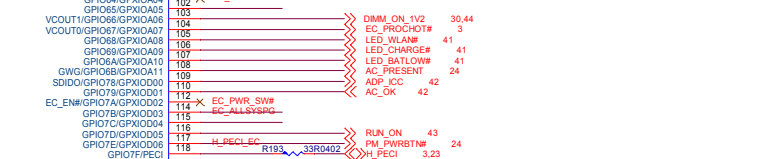
IEDI



## GPX10A



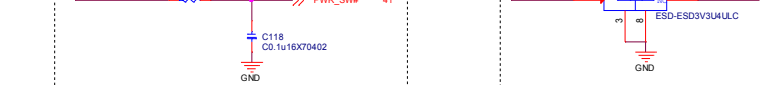
## POWER\_FAILON



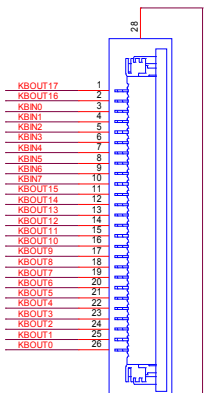
LED



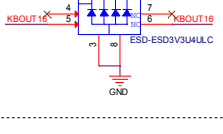
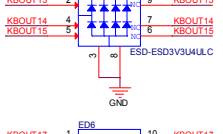
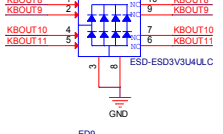
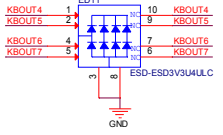
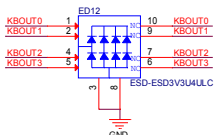
## E



## Keyboard conn



FPC26P-B-1PITCH\_WHITE  
N5A-26F0400-H06



PR140	R236	MB_ID
100K	NC	N17S-G1
NC	100K	UMA

**CPU FAN**

31,32 CPUFAN\_PWM

30mil

+5VRUN

GND

C473 X C1u6.3X60402

U31

1 FSM#

2 VIN

3 VOUT

4 VSET

8 GND

7 GND

6 GND

5 GND

VCCFAN1

R281 X 0R0402

X\_APL5606KI-TRL\_SOP8

122-0560602-A30

GND

31,32 CPUFAN\_PWM

+5VRUN

+3VRUN

C417 X\_C10u6.3X50603

C412 C1u6.3X60402

GND

GND

R14 10KR0402

R282 0R0402

C427 X\_C10u6.3X50603

GND

GND

GND

VCCFAN1

CON8

N32-1040430-H06

53261\_04

BH1X4HS-1.25PITCH\_WHITE

31 CPUFAN\_FB

**DGPU FAN**

30mil +5VVRUN

GND C175 X C1u6.3X60402

U3

1 FSM# GND 8

2 VIN GND 7

3 VOUT GND 6

4 VSET GND 5

X\_APL5606KI-TRL\_SOP8

VCCFAN2

31,32 GPUFAN\_PWM R38 X\_0R0402

**I22-0560602-A30**

GND

+5VVRUN

C447 X\_C10u6.3X50603

C449 X\_C1u6.3X60402

GND

+3VVRUN

R223 X\_10KR0402

GPUFAN\_FB 31

31,32 GPUFAN\_PWM R36 X\_0R0402 VCCFAN2

C434 X\_C10u6.3X50603

GND

GND

GND

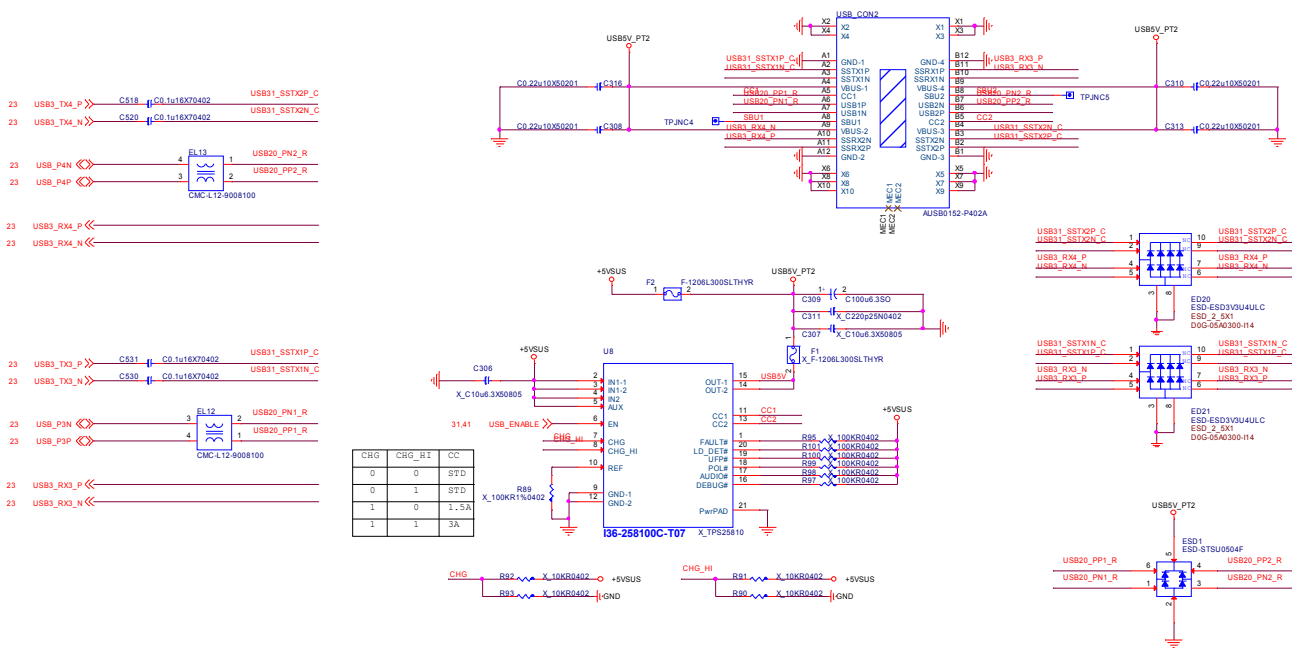
CON1

N32-1040430-H06

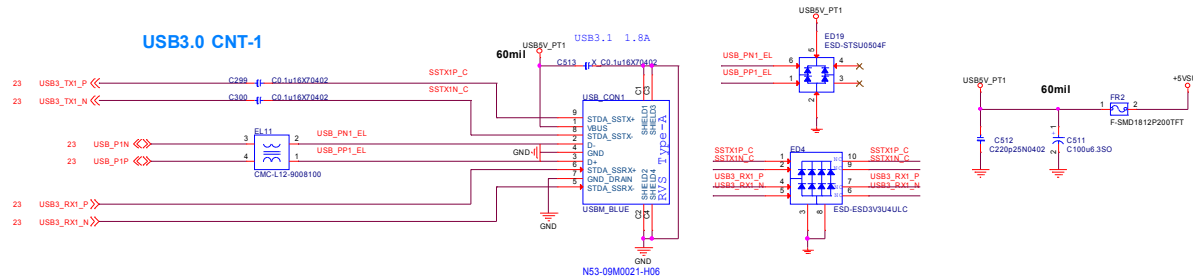
53261\_04

X\_BH1X4HS-1.25PITCH\_WHITE

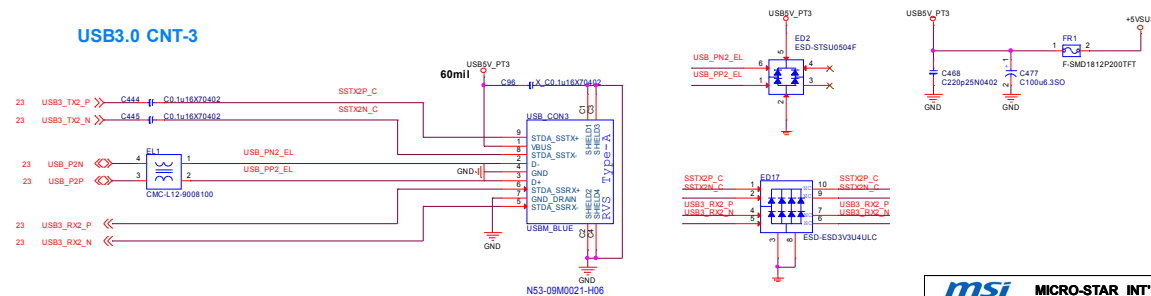
# USB 3.0 TYPE\_C



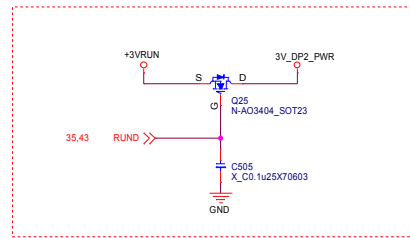
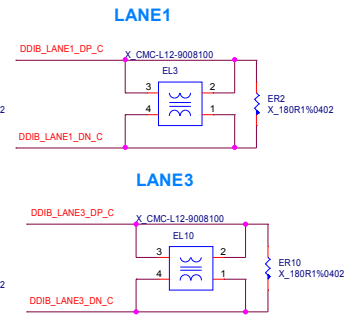
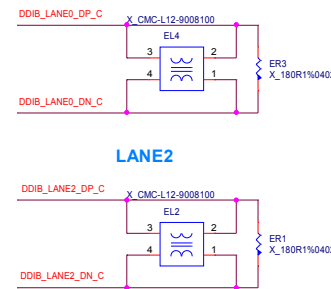
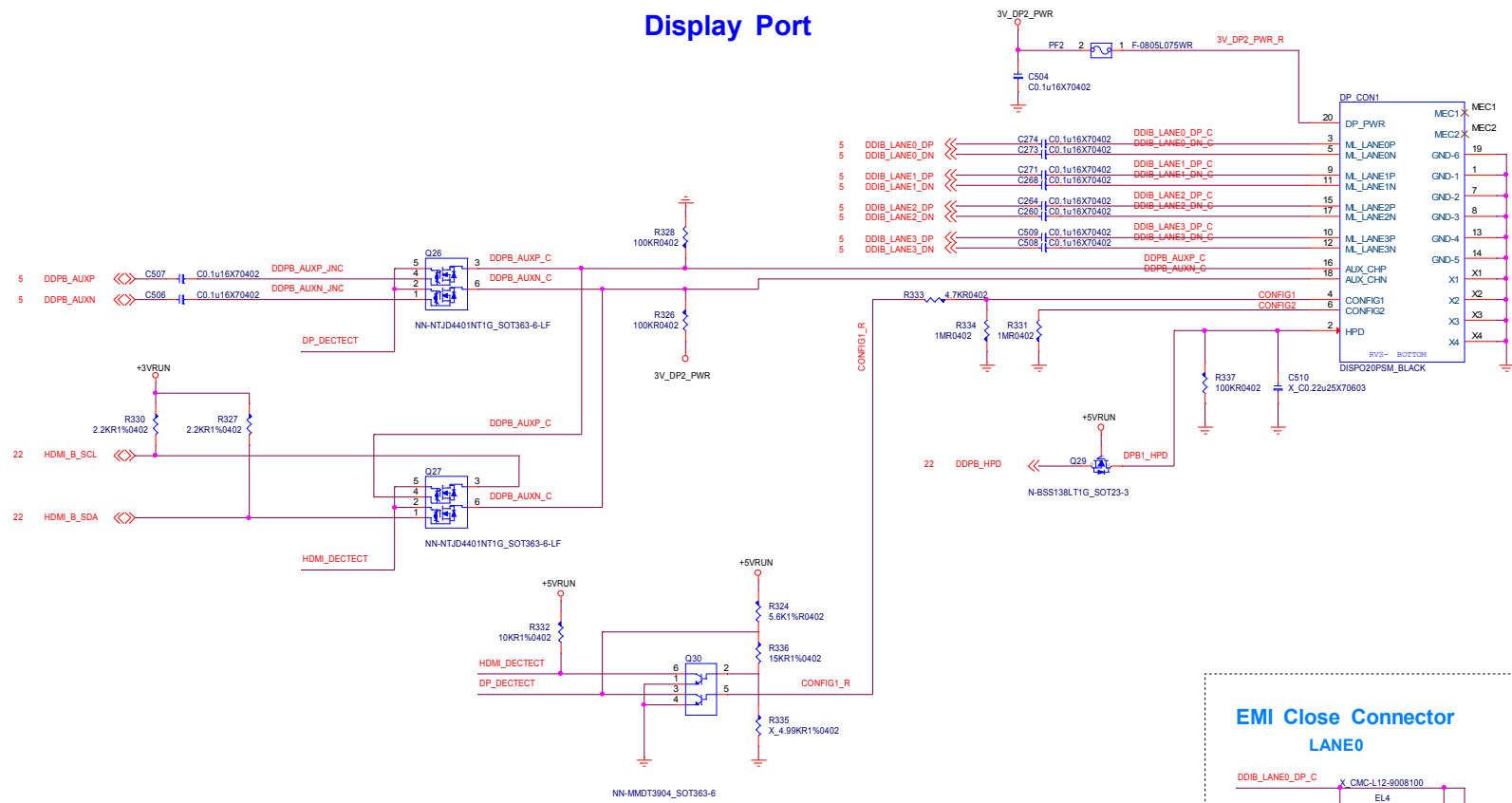
## USB3.0 CNT-1



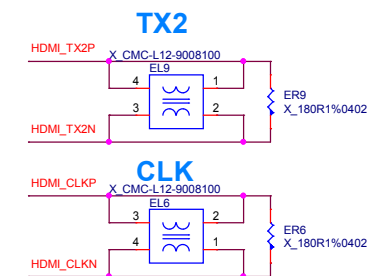
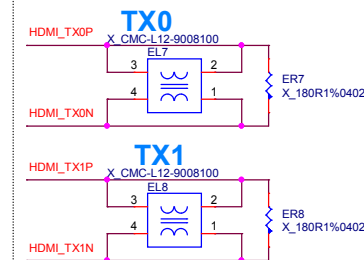
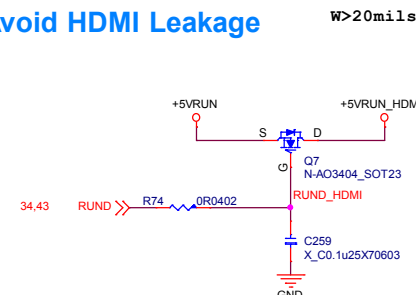
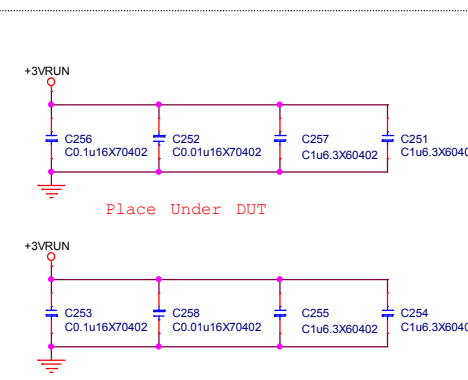
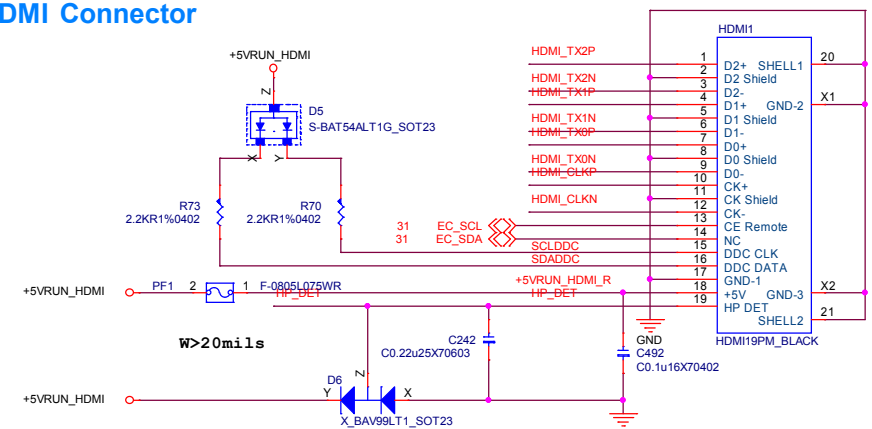
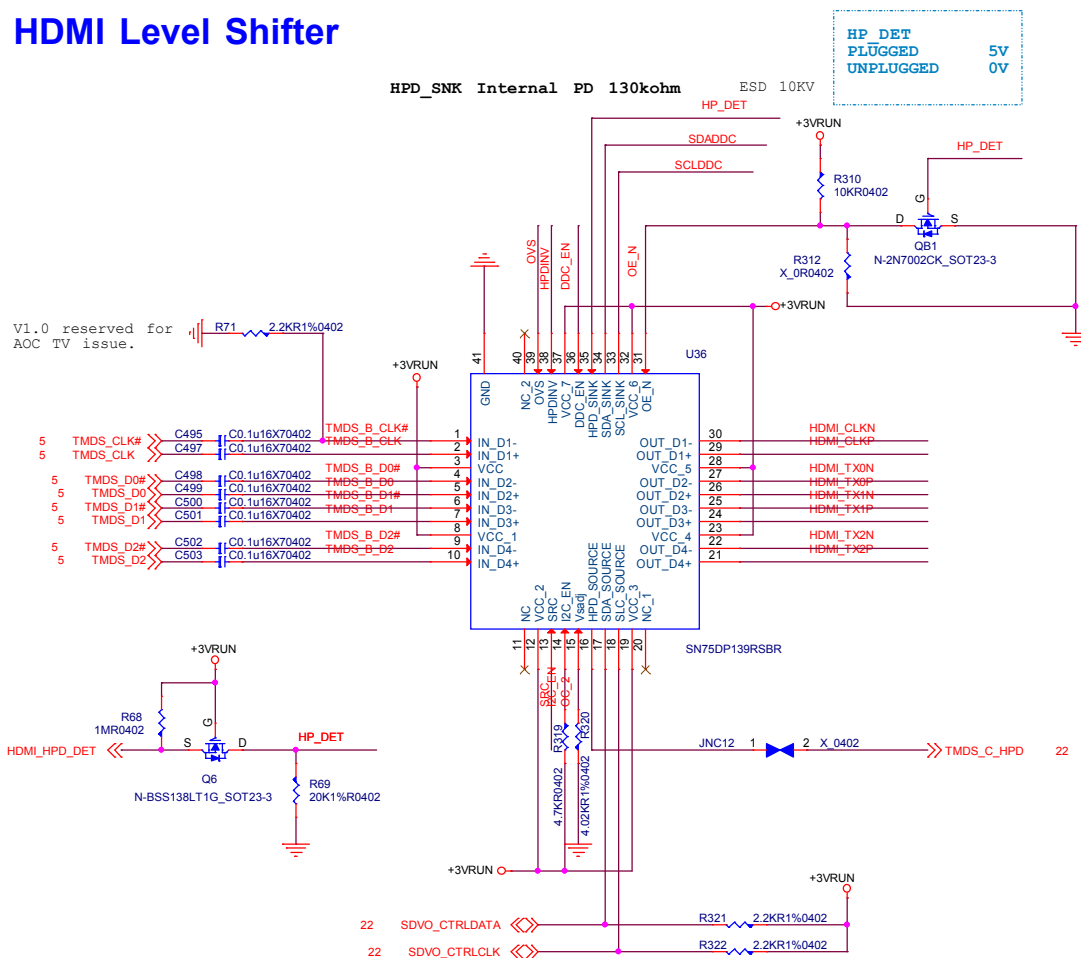
## USB3.0 CNT-3



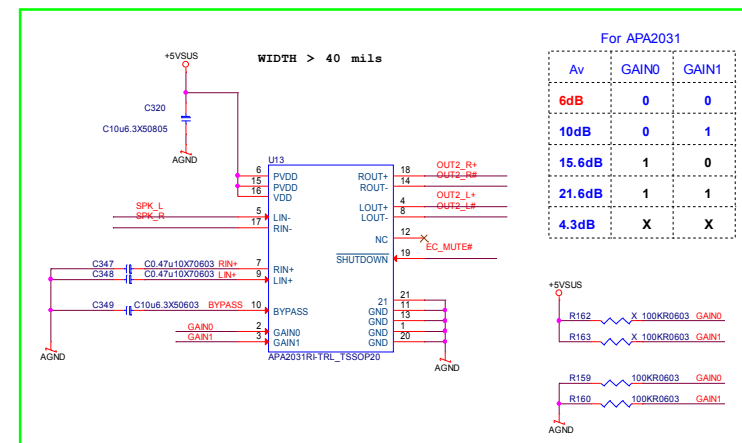
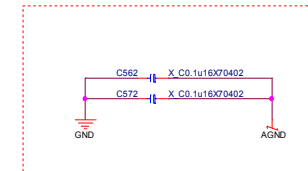
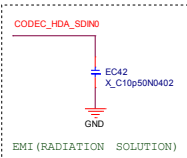
## Display Port



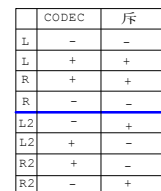
## HDMI Level Shifter



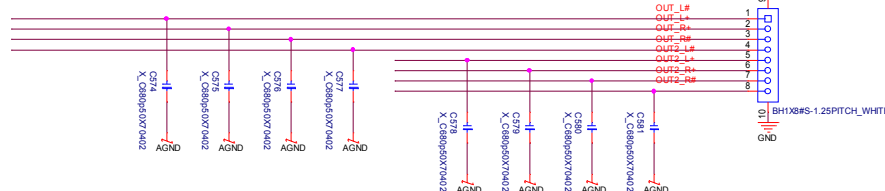
**Audio CODEC(ALC898/ALC892)/Audio AMP(APA2031)**



Av	GAIN0	GAIN1
6dB	0	0
10dB	0	1
15.6dB	1	0
21.6dB	1	1
4.3dB	X	X

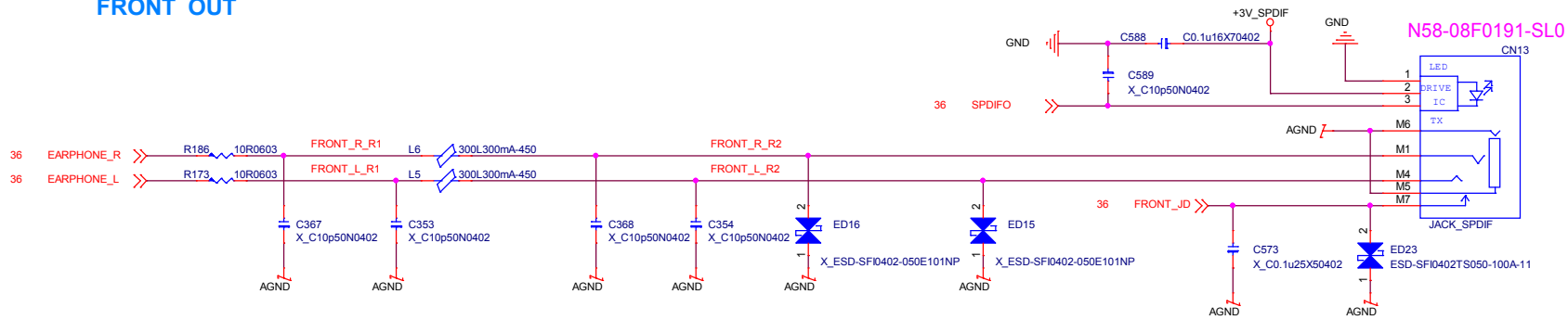


### Internal Speaker Conn

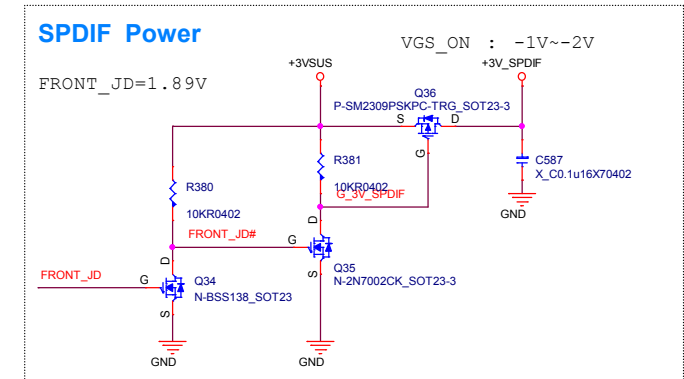
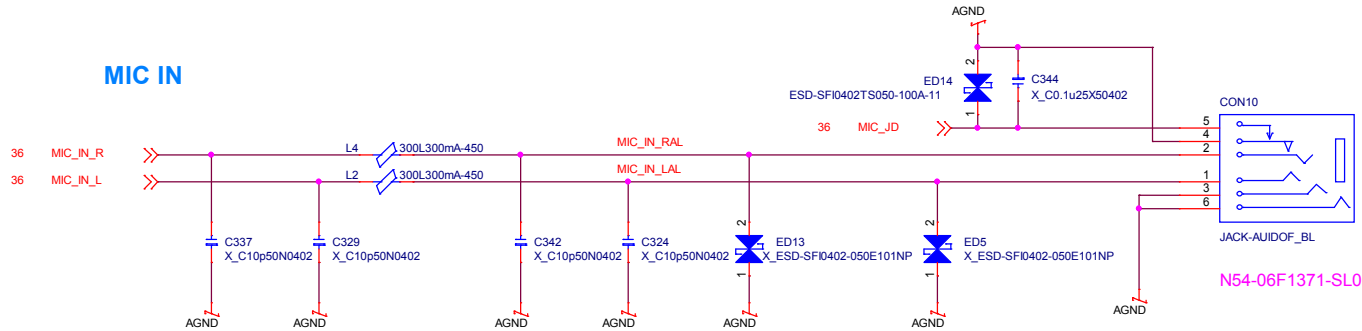


## Audio CONN

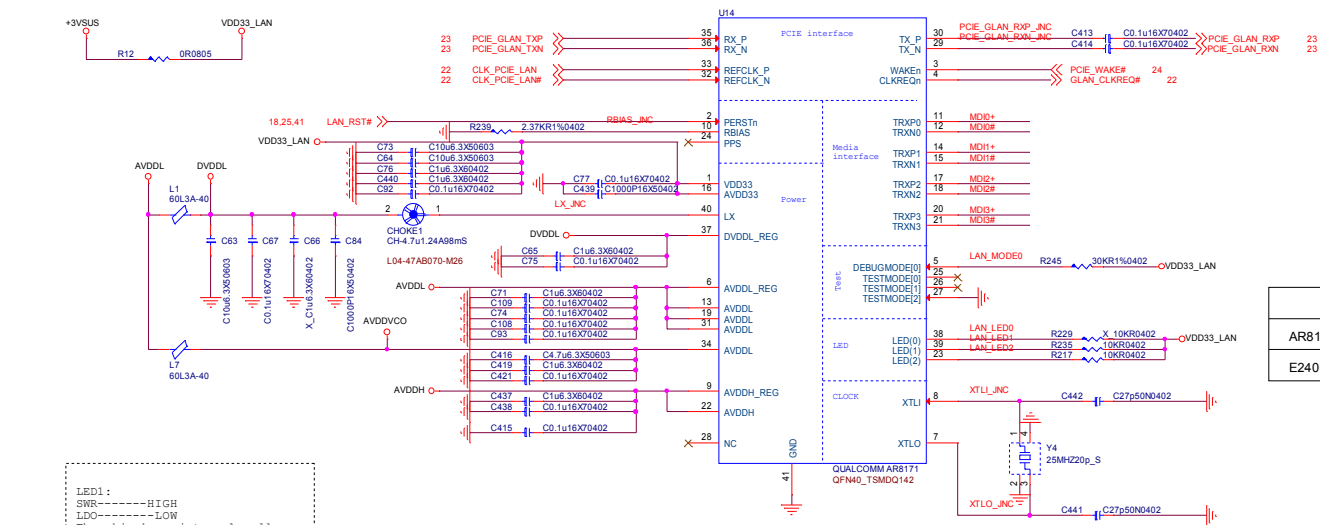
**FRONT OUT**



**MIC IN**



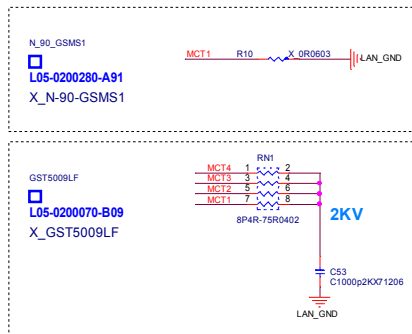
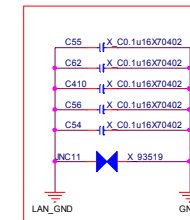
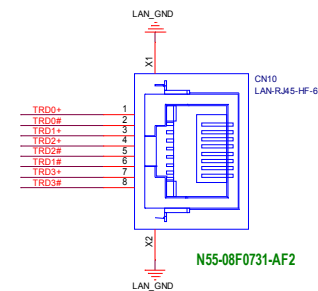
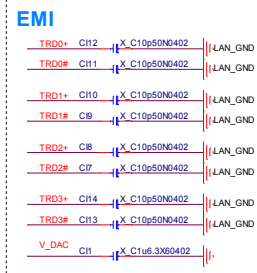
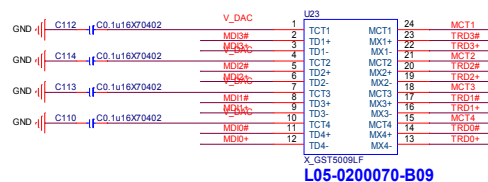
**GIGA LAN(BFN2400/AR8171)**



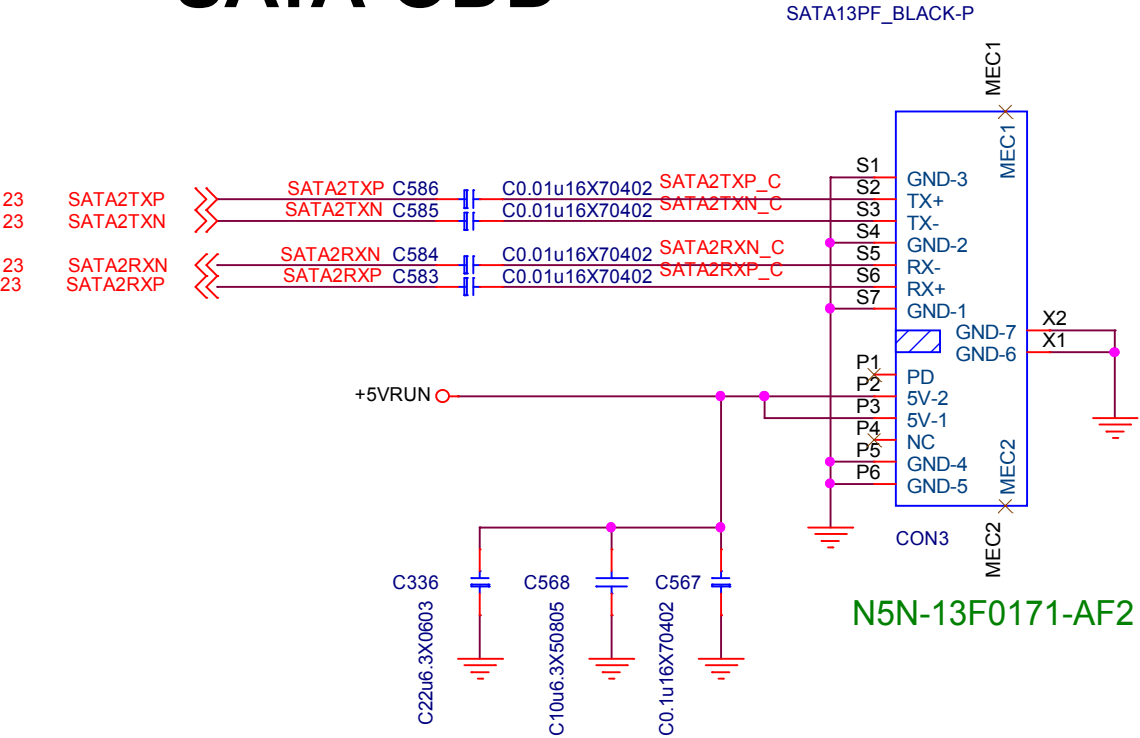
PIN 38 (LAN_LED0)	
AR8171	NC
E2400	Stuff

```
LED1:
SWR-----HIGH
LDO-----LOW
The chip have internal pull-up
```

```
LED2:
25MHz-----HIGH
48MHz-----LOW
The chip have internal pull-up
```

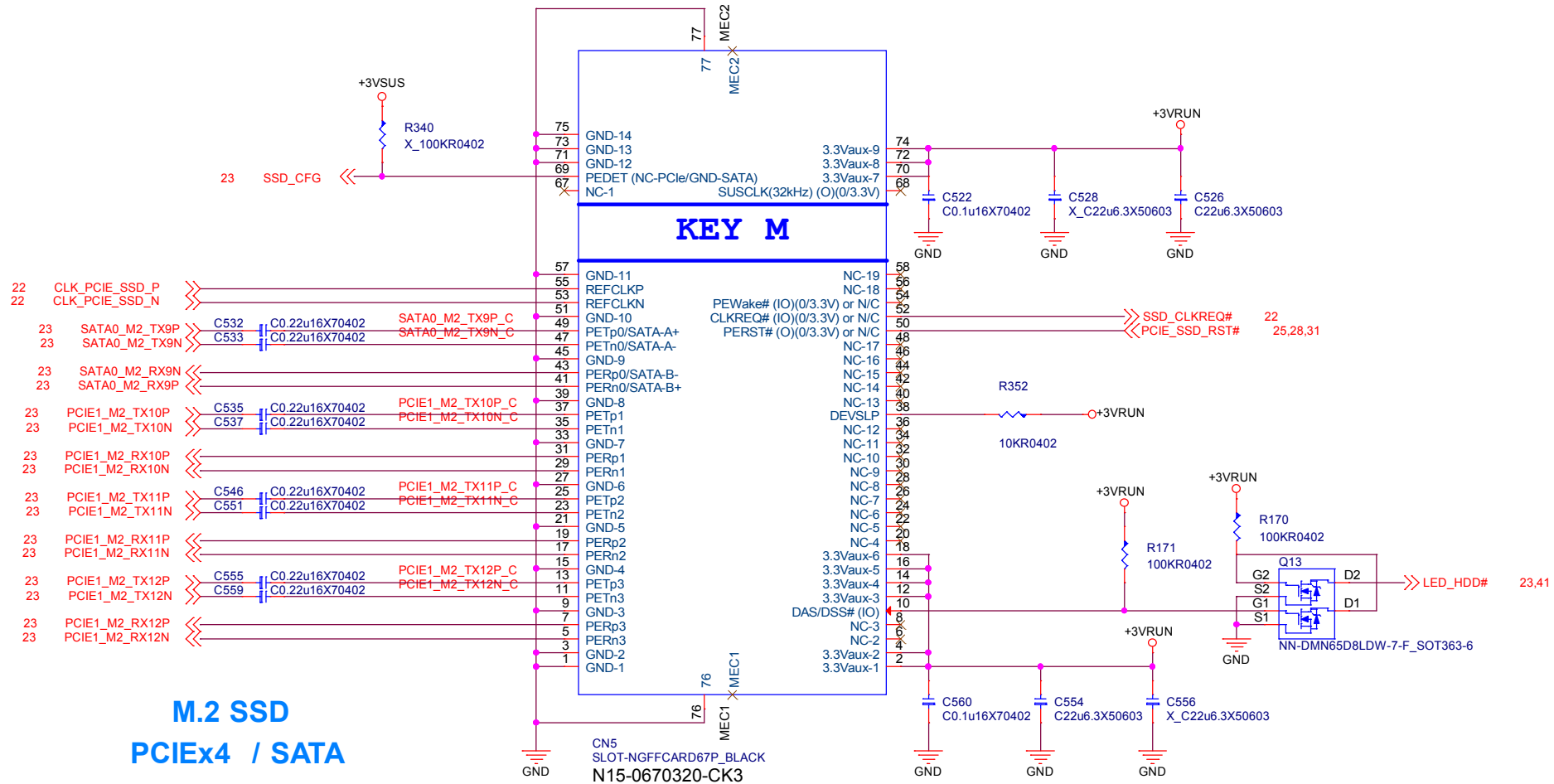


# SATA ODD



Title			
ODD			
Size A	Document	Number	Rev 0A
Date:	Thursday, May 23, 2017	Sheet 39 of 60	

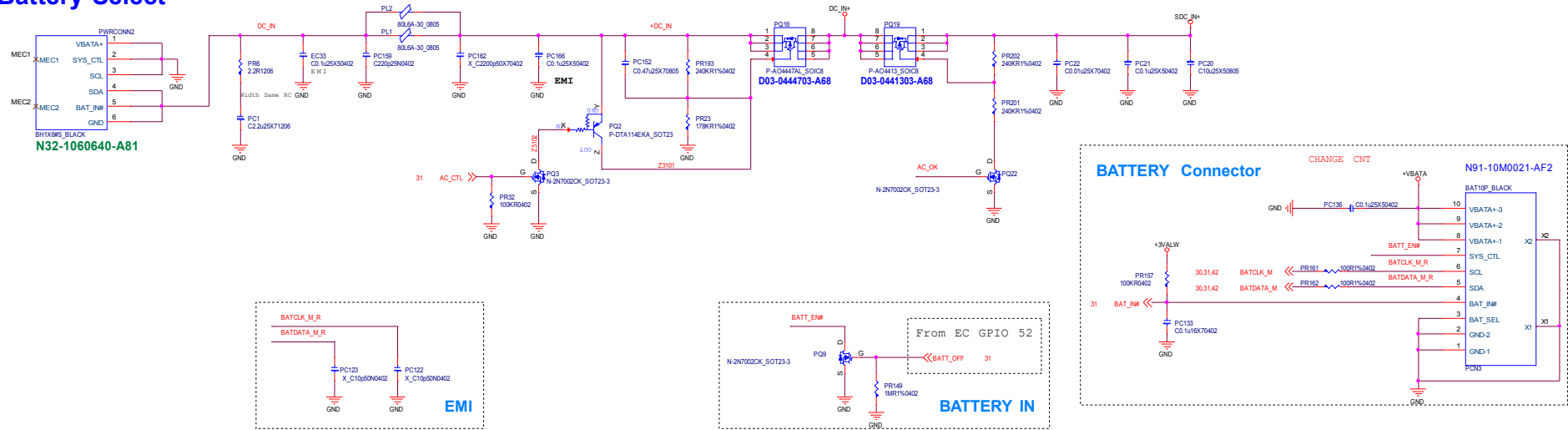
# SSD



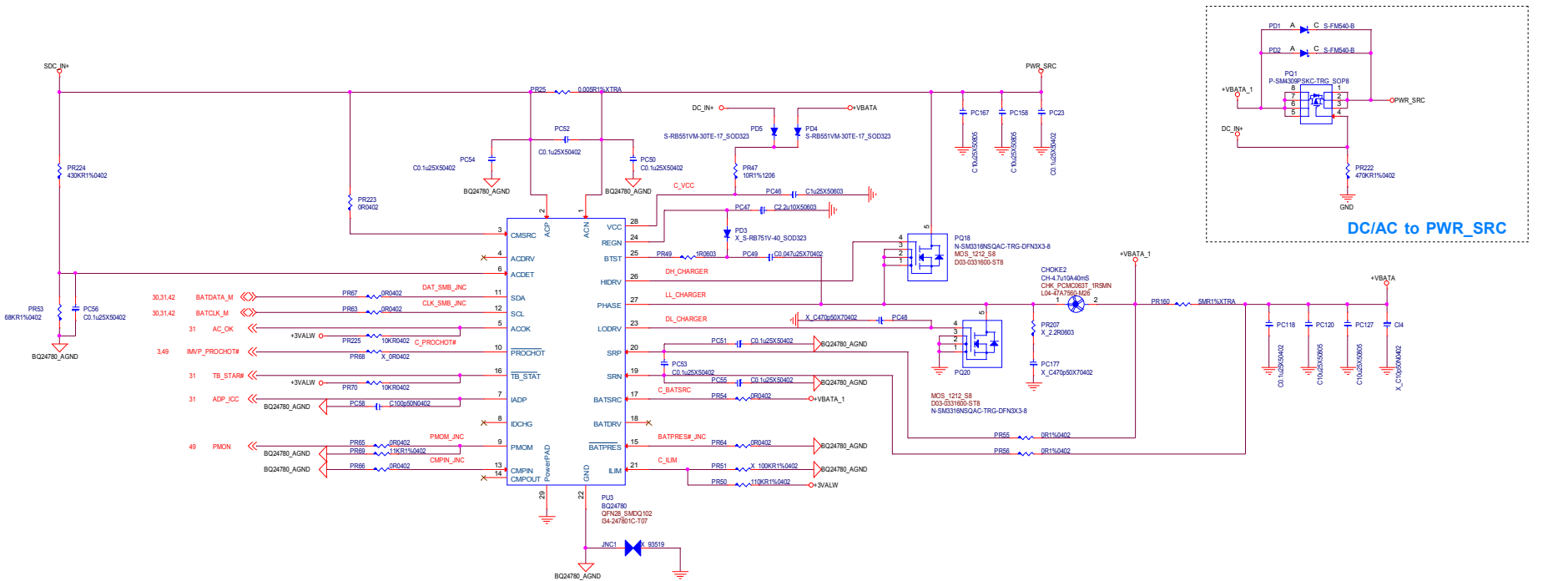


# Battery Select/Charger

## Battery Select



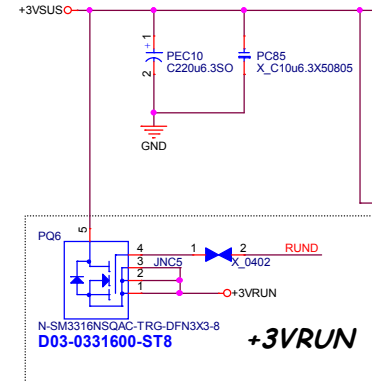
## Battery Charger



# System Power

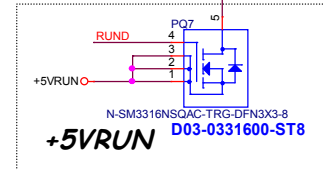
**OCF 13A  
MAX 10A**

**+3VSUS**

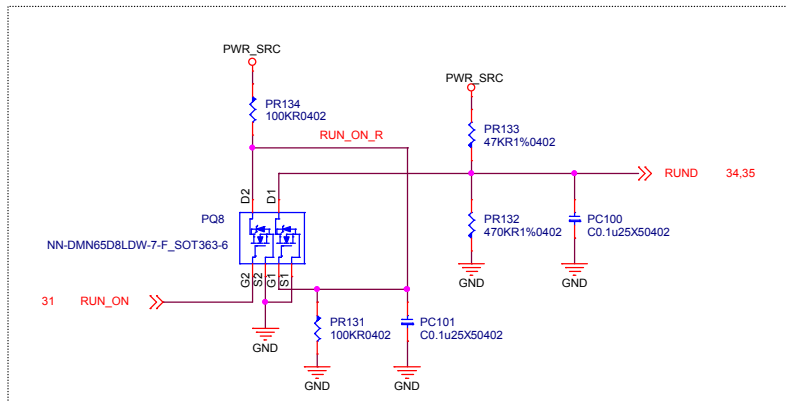


**OCF 12A  
MAX 9A**

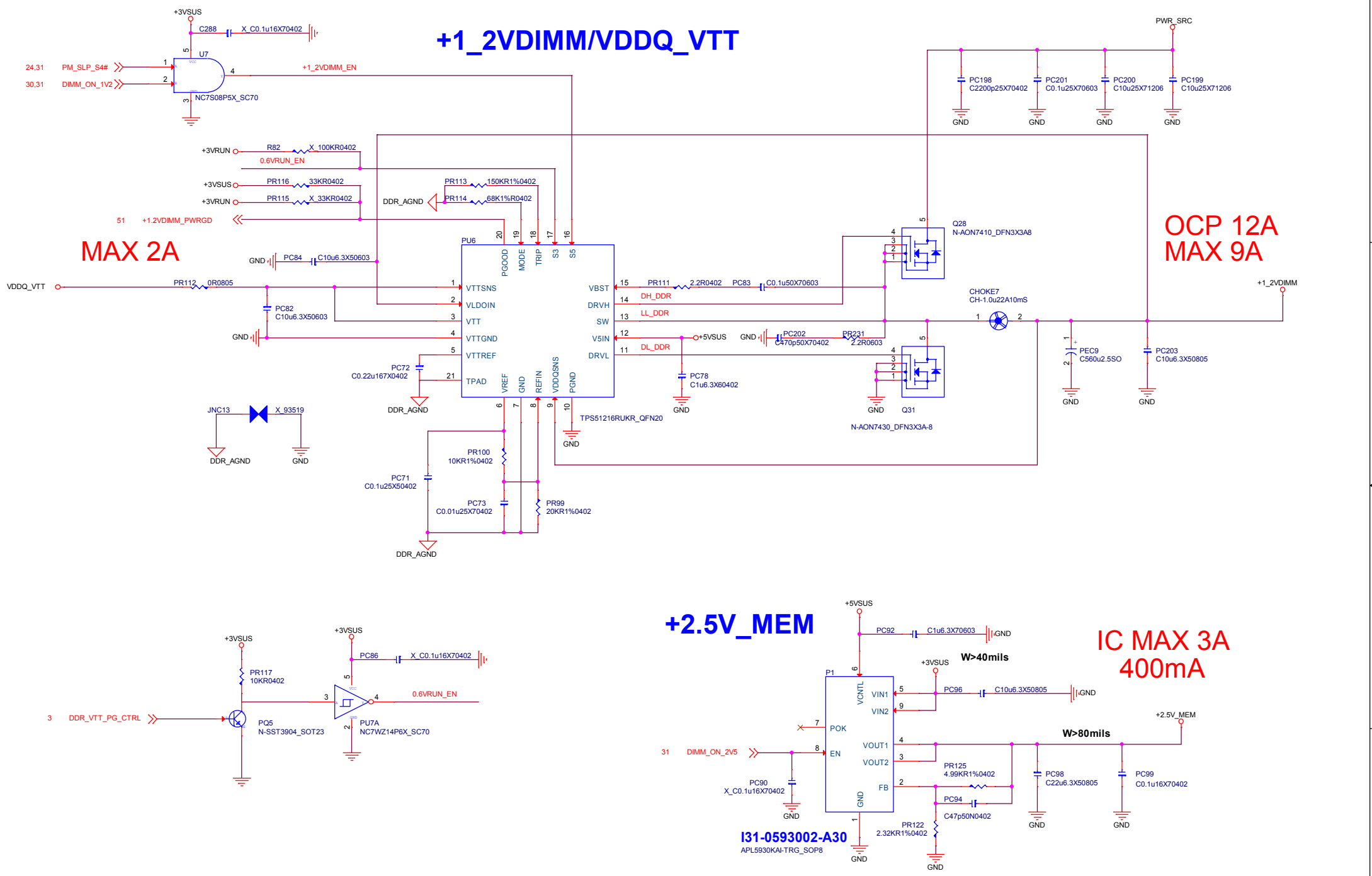
**+5VSUS**



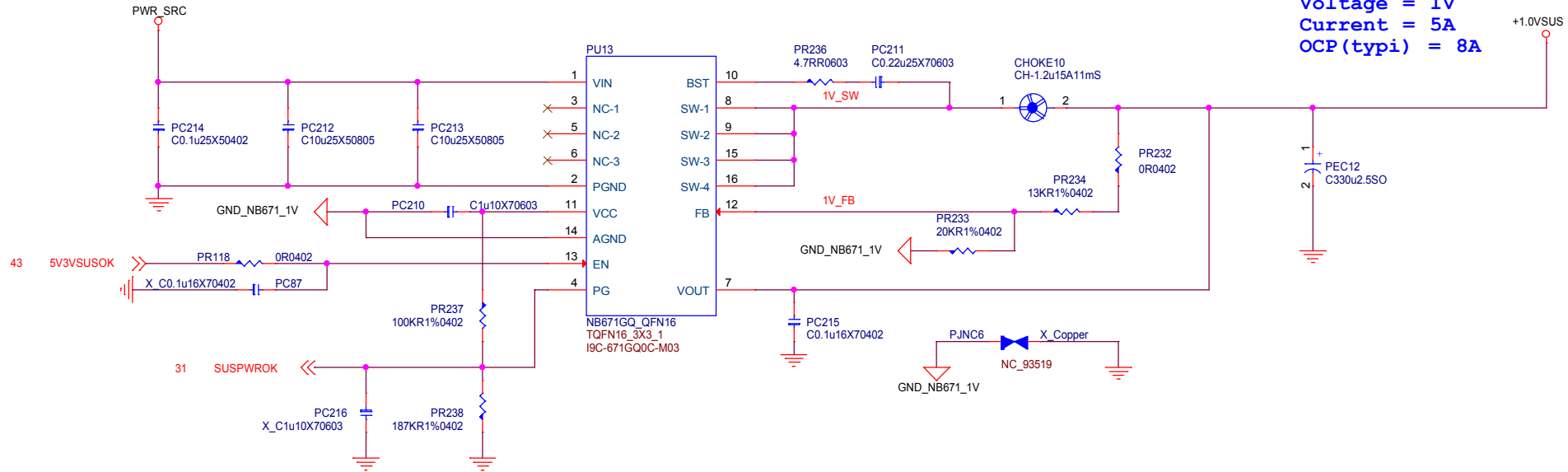
**+3VALW** **+5VALW**



<b>msi</b> MICRO-STAR INT'L CO.,LTD.	
Title	
<b>System Power</b>	
Size	Document Number
<b>MS-16JD</b>	
Date:	Thursday, March 23, 2017
Sheet	43 of 60
Rev	0A

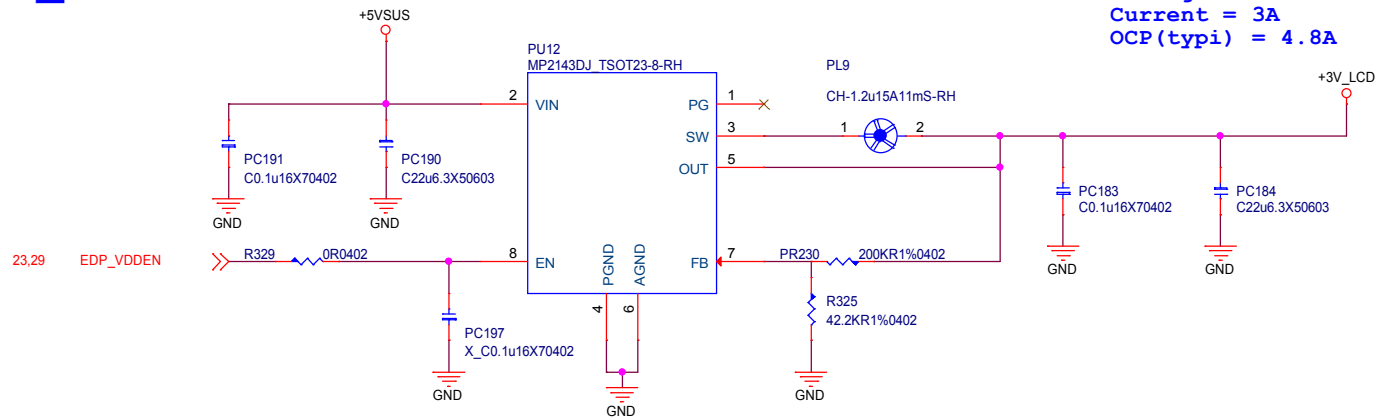


# +1VSUS

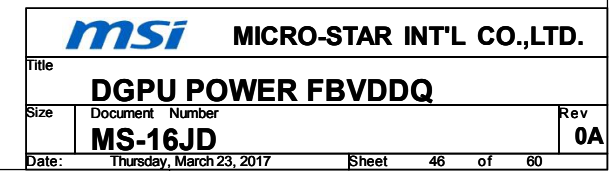


# +3V\_LCD

## Panel Device Logic Power

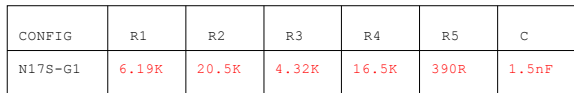


**FBVDDQ**  
**OCP 11A**  
**MAX 9A**

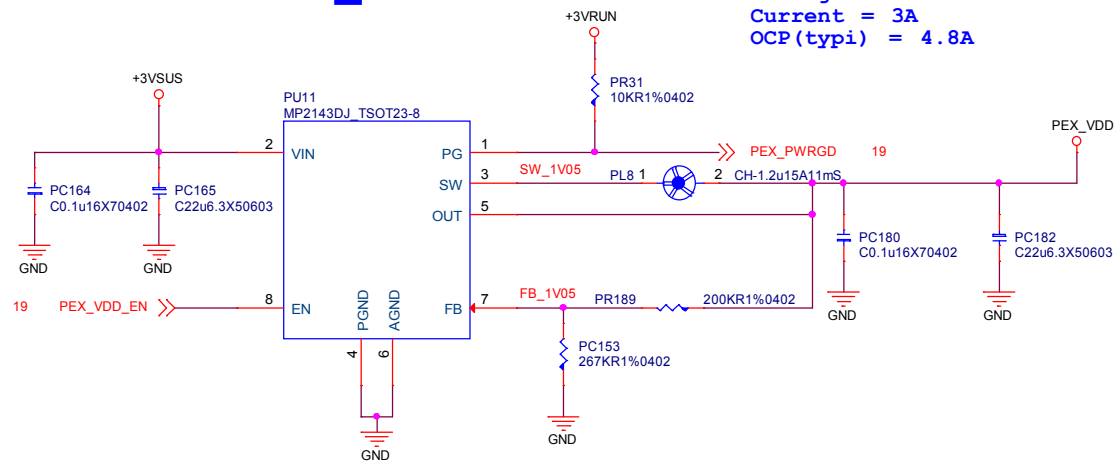


## EDP-Con 50A

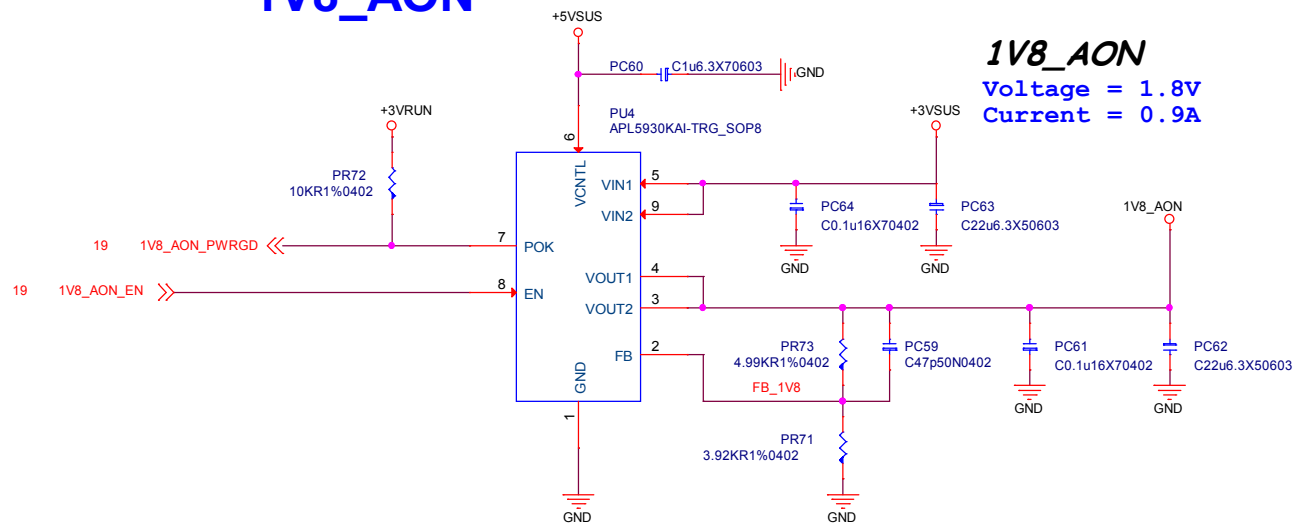
**Vmin:0.6V / Vmax:1.2V**




# PEX\_VDD



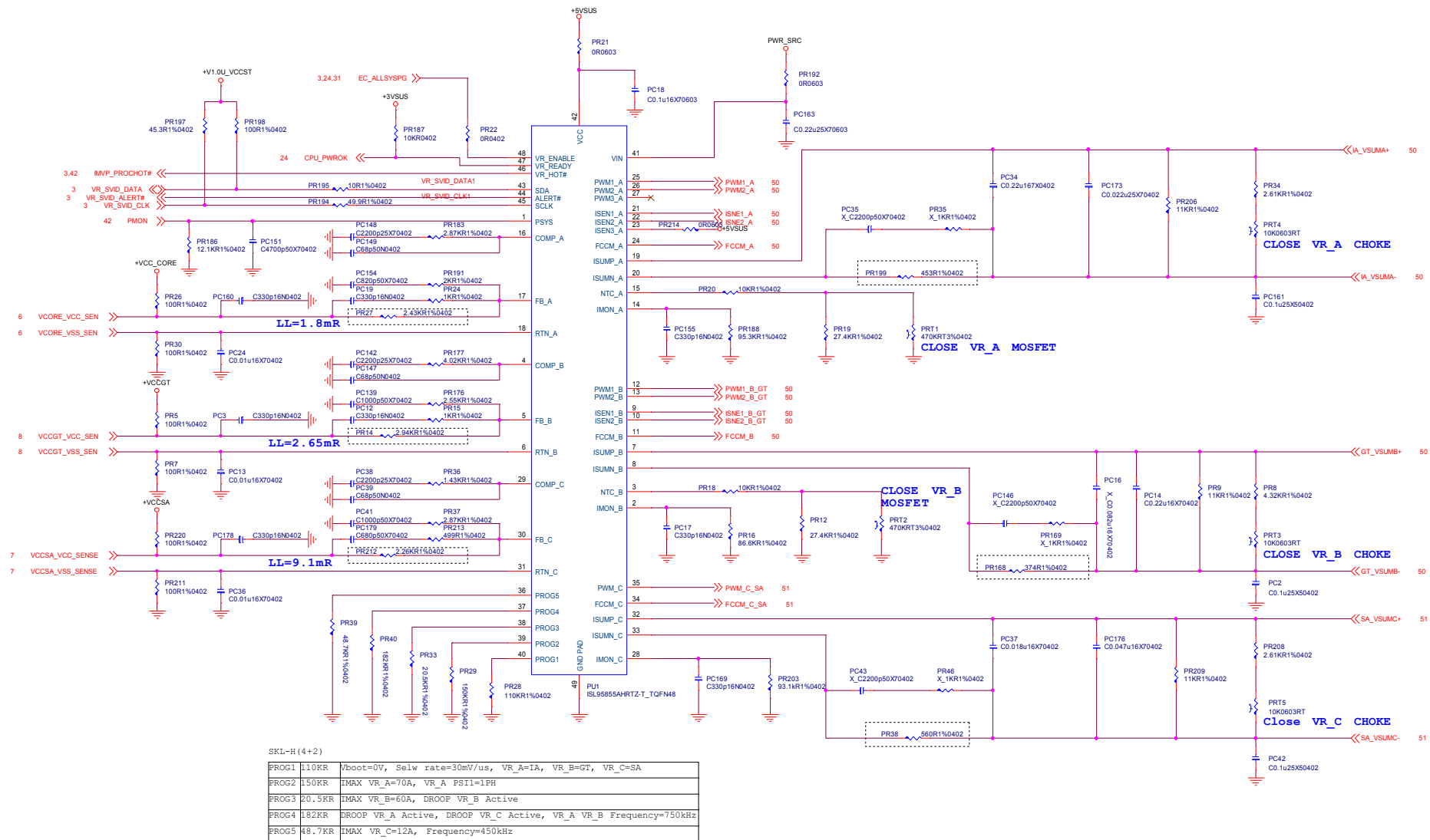
# 1V8\_AON

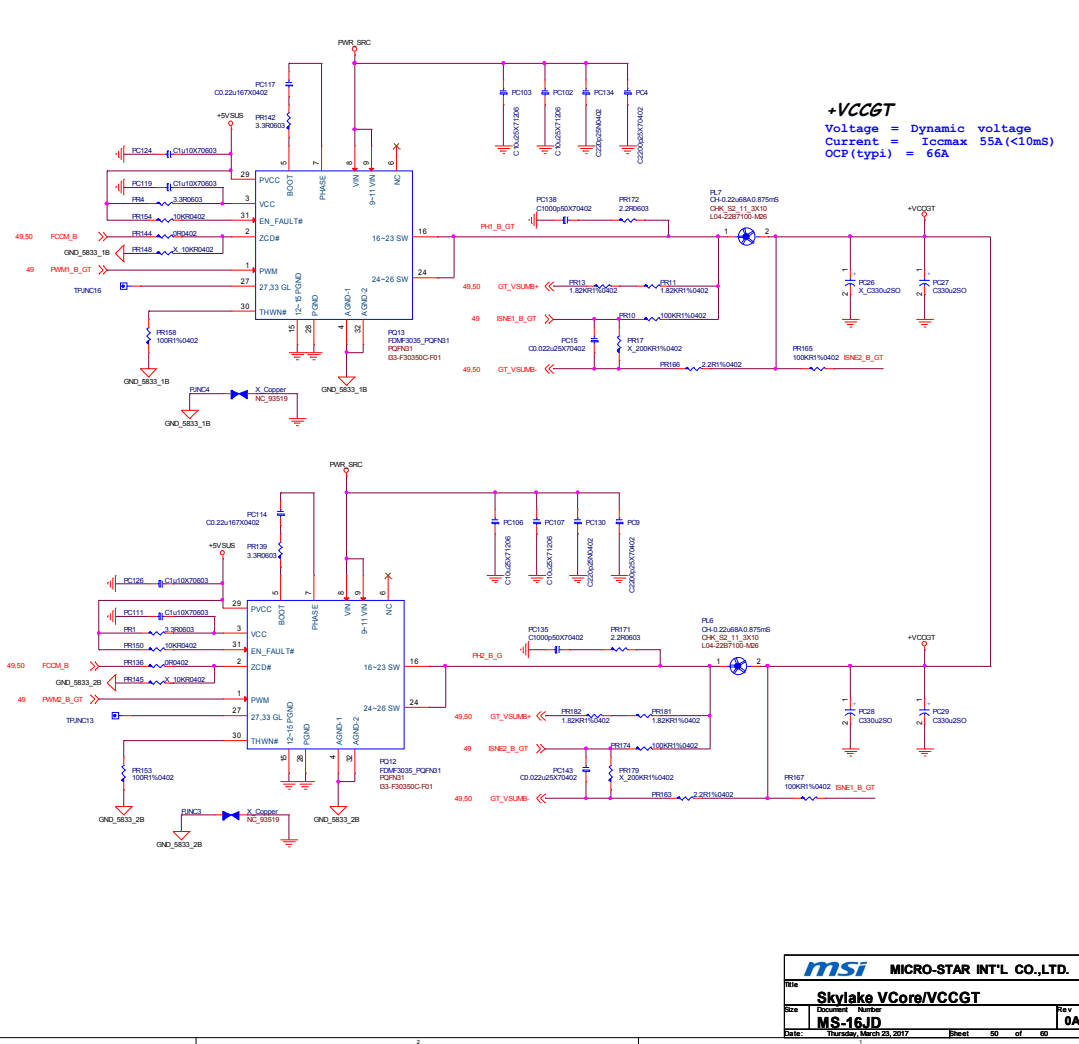
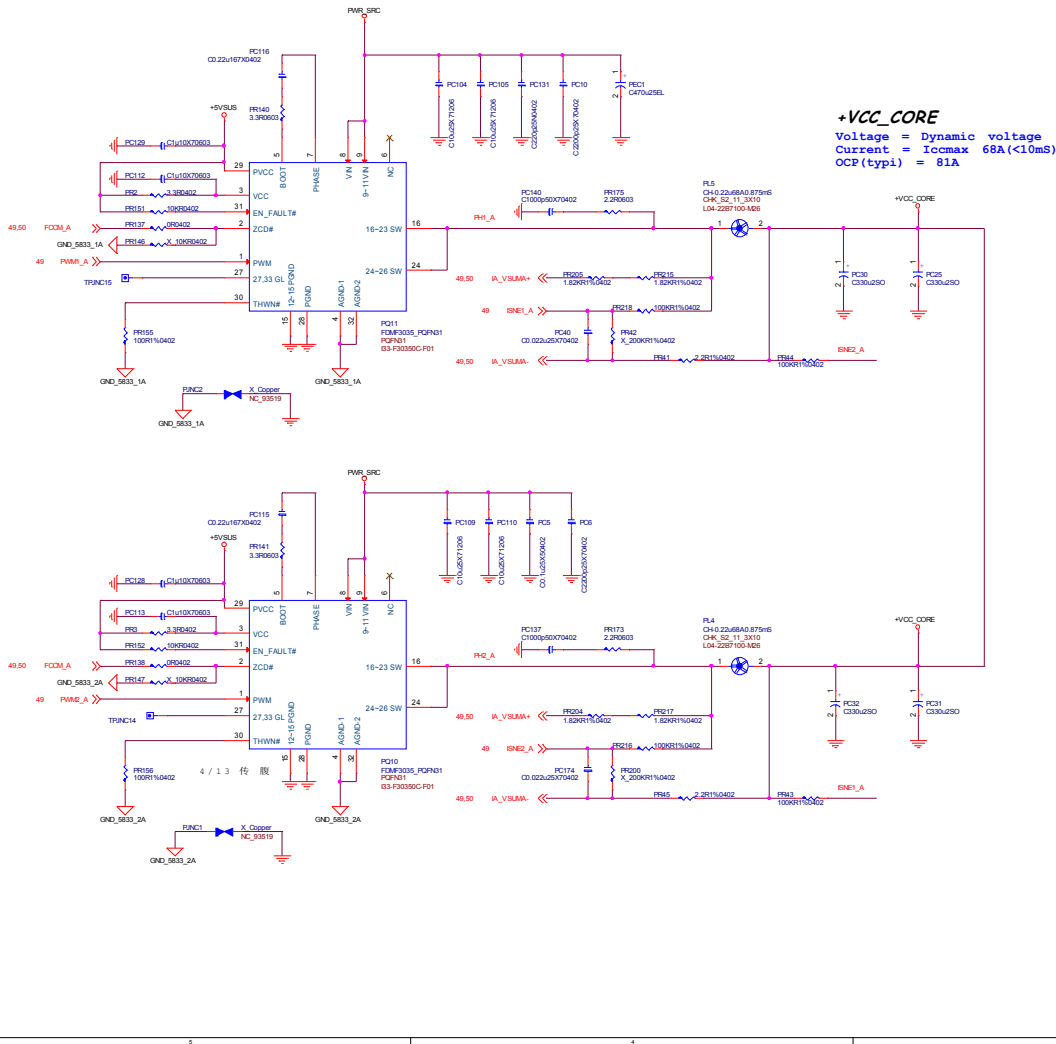


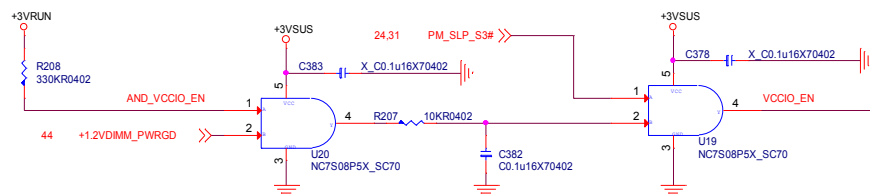
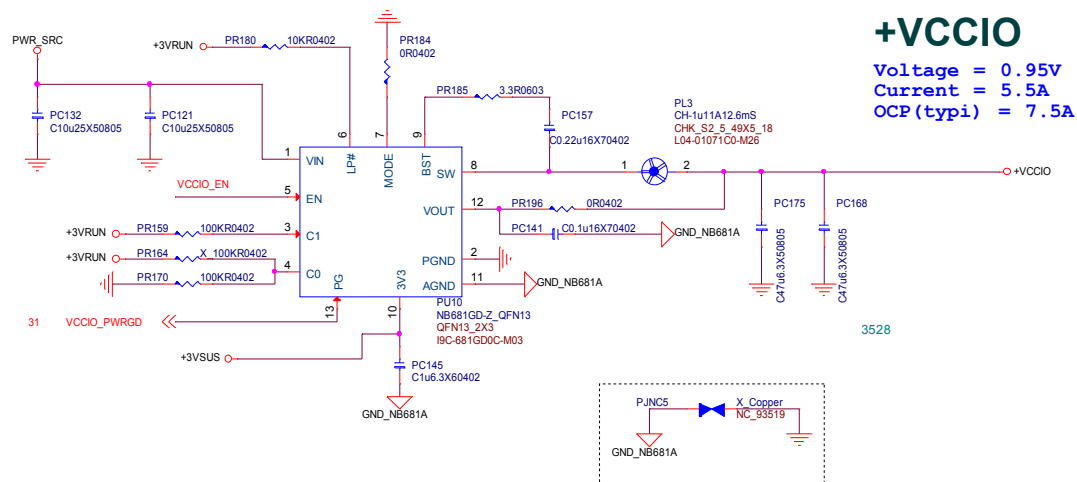
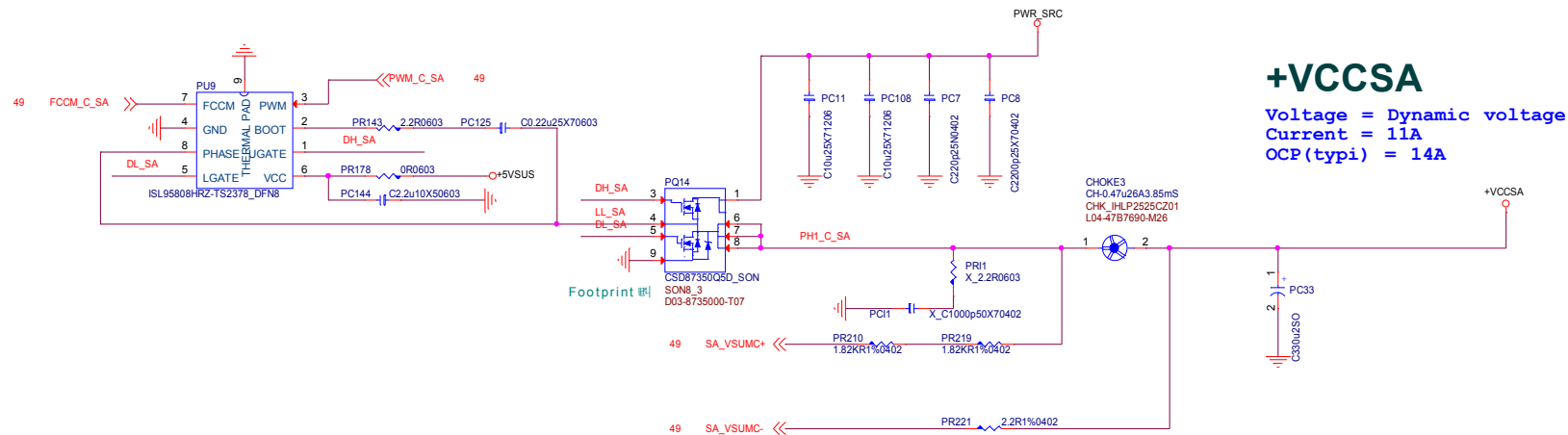
2016/02/17 Modify PR255 3.92Kohm for Power suggestion

		MICRO-STAR INT'L CO.,LTD.	
Title <b>DGPU POWER PEX_VDD / 1V8_AON</b>			
Size	Document	Number	Rev
	<b>MS-16JD</b>		<b>0A</b>
Date:	Thursday, March 23, 2017		Sheet 48 of 60

## Skylake H-line 42 45W ISL95855



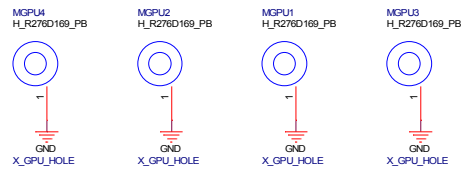






The diagrams illustrate the connection of four MCPUs to a common ground:

- MCPU4**: H\_R276D169\_PB. The red line connects the bottom terminal to the ground symbol.
- MCPU2**: H\_R276D169\_PB. The red line connects the bottom terminal to the ground symbol.
- MCPU3**: H\_R276D169\_PB. The red line connects the bottom terminal to the ground symbol.
- MCPU1**: H\_R276D169\_PB. The red line connects the bottom terminal to the ground symbol.



BRACKET1

CPU BKT

CPU\_BRACKET

**E2M-7810111-A89**

BRACKET2

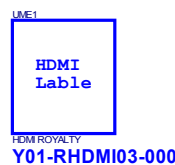
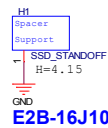
GPU BKT

GPU\_BRACKET

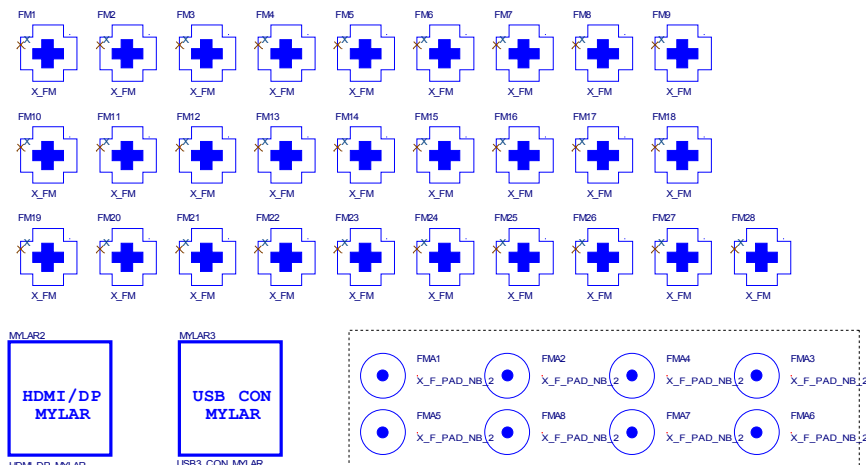
**307-6J30111-HG0**

H2  
Spacer  
Support  
1 SSD\_STANDOFF  
H=4.15  
GND  
**E2B-16J1010-A89**

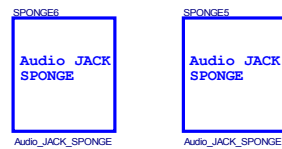
H1  
Spacer  
Support  
SSD\_STANDOFF  
H=4.15



Hannstar: P30-16J6111-H73  
TRIPOD: P30-16J6111-T53



E2M-3570611-Y42 E2M-3570611-Y42

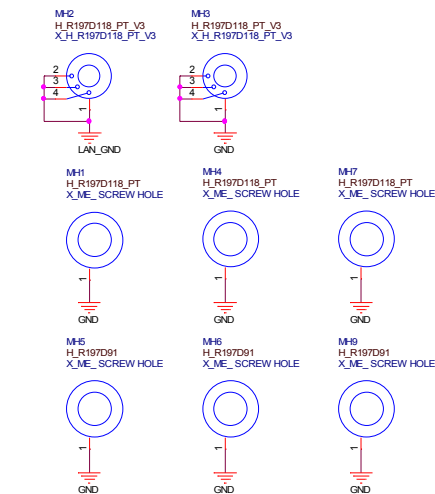
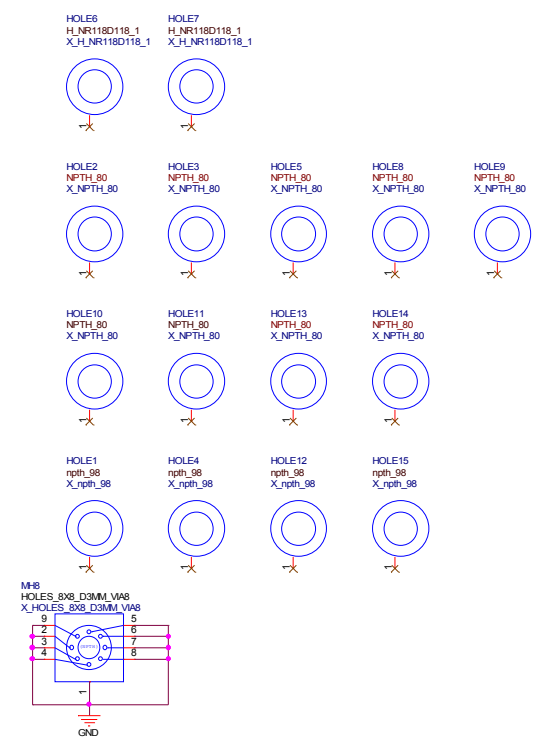


E2Y-X047411-CA7 E2Y-X047411-CA7

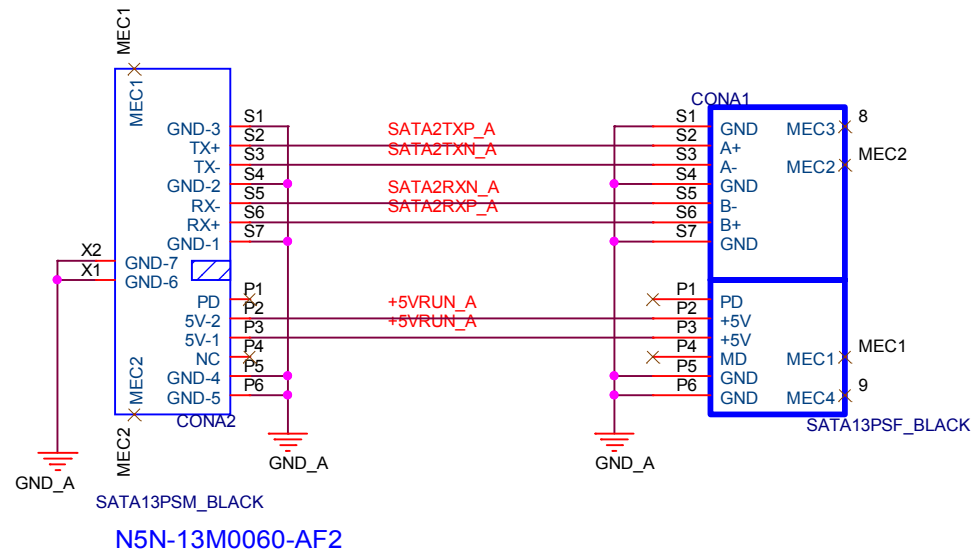
Figure 1 shows three examples of LED identification. The first example, labeled 'MYLARS', shows a blue square with 'ME\_MYLAR' text. The second example, labeled 'SPONGE1', shows a blue square with 'LED SPONGE' text. The third example, labeled 'SPONGE2', shows a blue square with 'LED SPONGE' text. Below each example is a label: 'Hide\_Caps\_Lock\_LED\_MYLAR' for the first, 'LED\_SPONGE' for the second, and 'LED\_SPONGE' for the third. At the bottom of each column is a yellowed label: 'E2Y-6324111-Y42' for the first, 'E2Y-6J10611-Y42' for the second, and 'E2Y-6J10611-Y42' for the third.

Diagram showing four square components labeled MYLAR6, MYLAR7, MYLAR8, and SPONGE4. MYLAR6, MYLAR7, and MYLAR8 are labeled "MB MYLAR" and are connected to "X\_MB MYLAR". SPONGE4 is labeled "LED SPONGE" and is connected to "X\_LED\_SPONGE".

**E2P-7910312-G40    E2P-0113511-G40    E2P-7910811-G40    E2Y-7910211-G40**



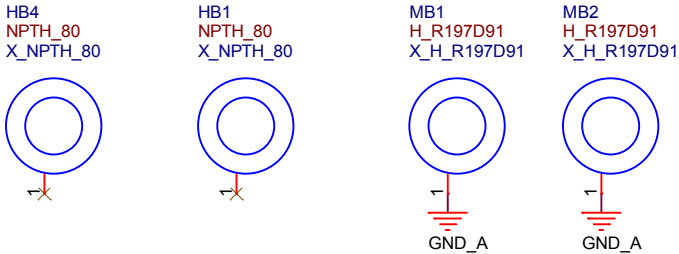
179D-A Board (ODD)



**PCBA1**

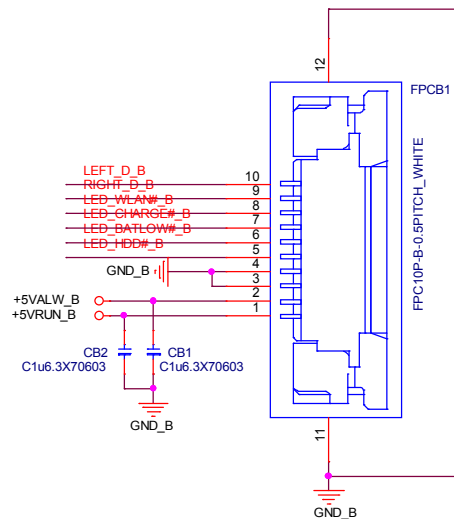
PD0-16JDA0A-H73  
**PD0-16JDA0A-H73**

Hannstar: PD0-16JDA0A-H73  
TRIPOD: PD0-16JDA0A-T53



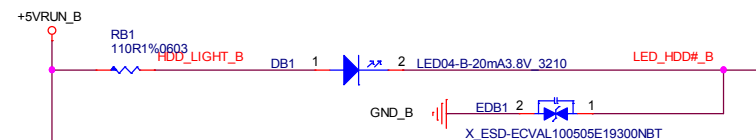
**E43-1205003-H29      E43-1205003-H29**

# 179D-B Board (LED / TP)

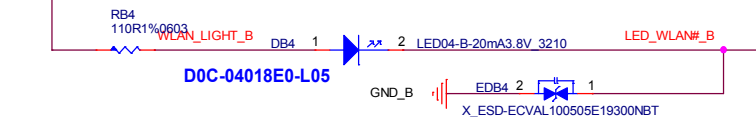


## LED FRONT

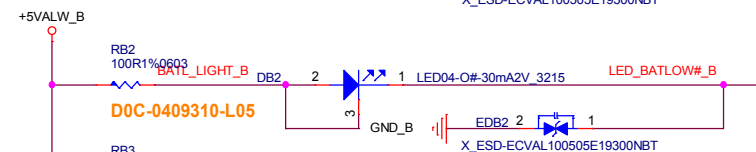
BLUE  
(HDD)



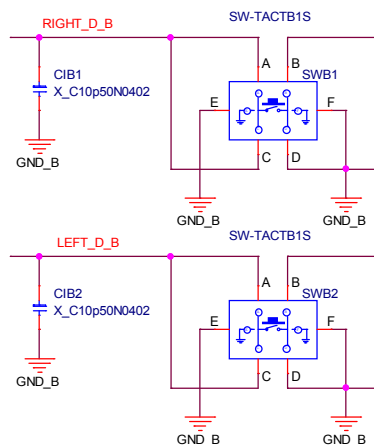
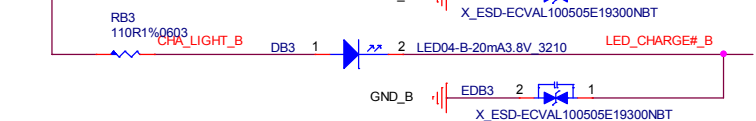
BLUE  
(WLAN)



ORANGE  
(BATLOW)

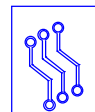


BLUE  
(CHARGE)



H=1.5mm

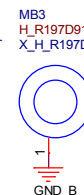
PCBB1



PD0-16JDB0A-H73

PD0-16JDB0A-H73

Hannstar: PD0-16JDB0A-H73  
TRIPOD: PD0-16JDB0A-T53



msi

MICRO-STAR INT'L CO.,LTD.

Title

[B] 179D LED / TP

Size

Document Number

MS-16JD

Rev

0A

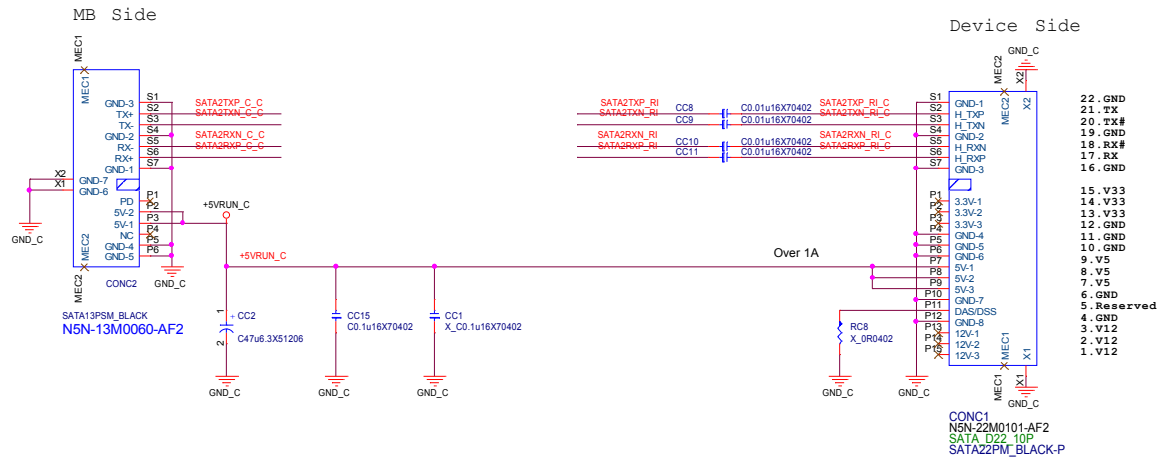
Date:

Thursday, March 23, 2017

Sheet

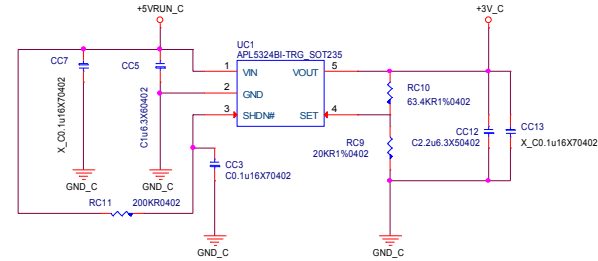
55 of 60

# 16JD-C Board (ODD TO HDD)

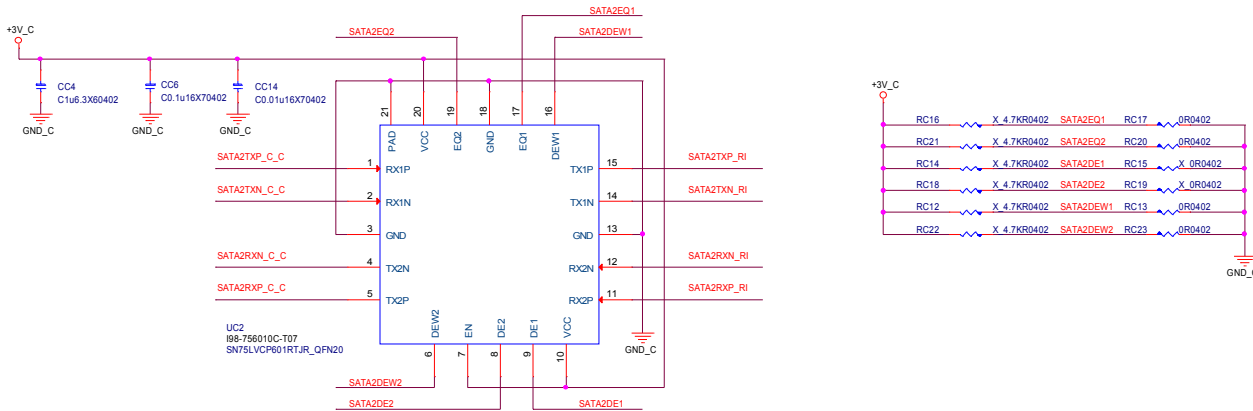


3.3V

Voltage = 3.3V  
Current = 0.1A



## SATA ReDriver



## TI SN75LVCP601RTJR HW Setting

DE1/DE2	CH1/CH2De-Emphasis dB (at 6Gbps)	DQ1/DQ2	CH1/CH2De-Emphasis dB (at 6Gbps)
NC(default)	-4	NC(default)	0
0	0	0	7
1	-2	1	14

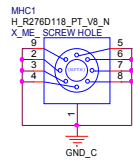
DEW1/DEW2	Device Function --> De Width for CH1/CH2
0	De-emphasis Pulse duration, short(recommended setting when linkoperates at SATA 1.5/3/6 Gbps)
1(default)	De-emphasis Pulse duration, long(recommended setting when linkoperates at SATA 1.5/3/6 Gbps)

### PCBC1

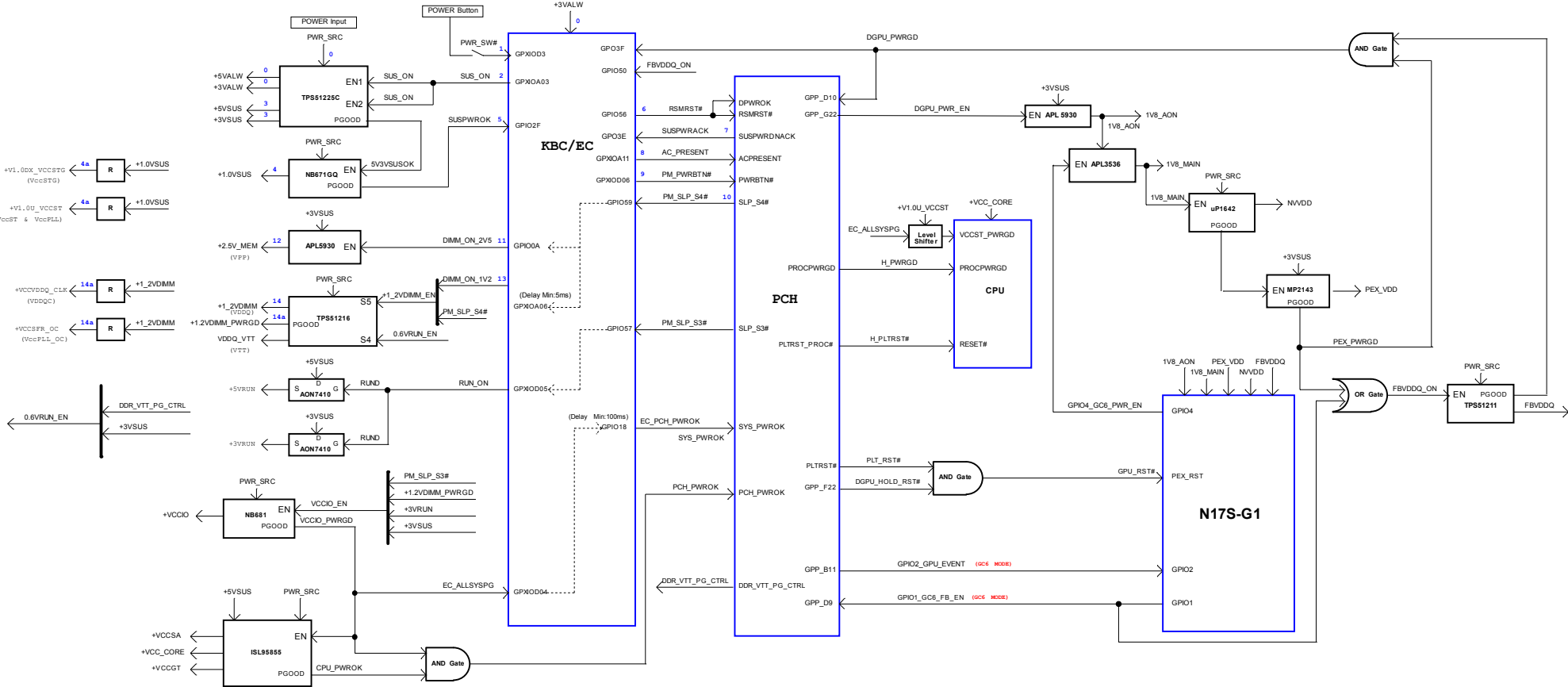


PD0-16JDC0A-H73

Hannstar: PD0-16JDC0A-H73  
TRIPOD: PD0-16JDC0A-T53

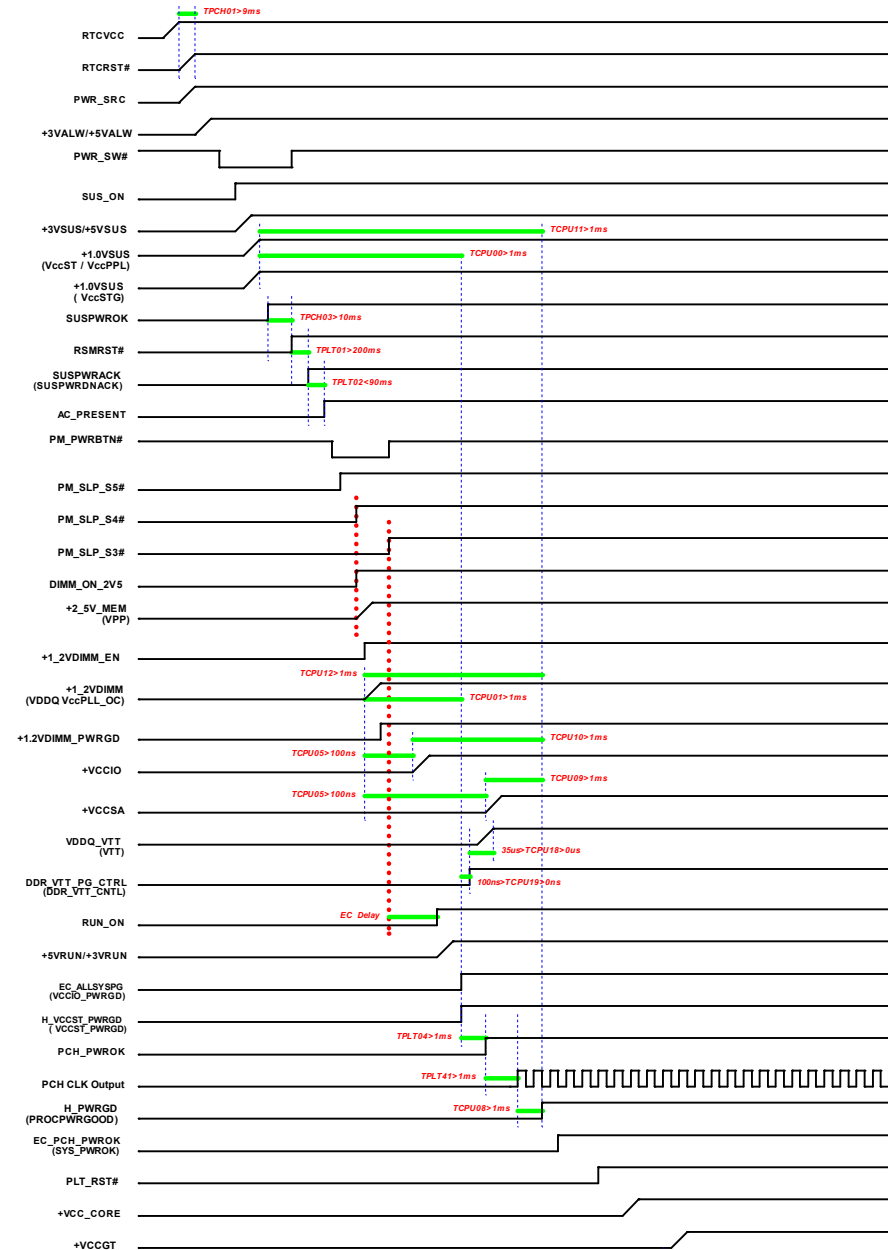


## MS-16JD Power on Block Diagram



# Power on Sequence

G3 -> S0



# Power Down Sequence

S0 -> G3

